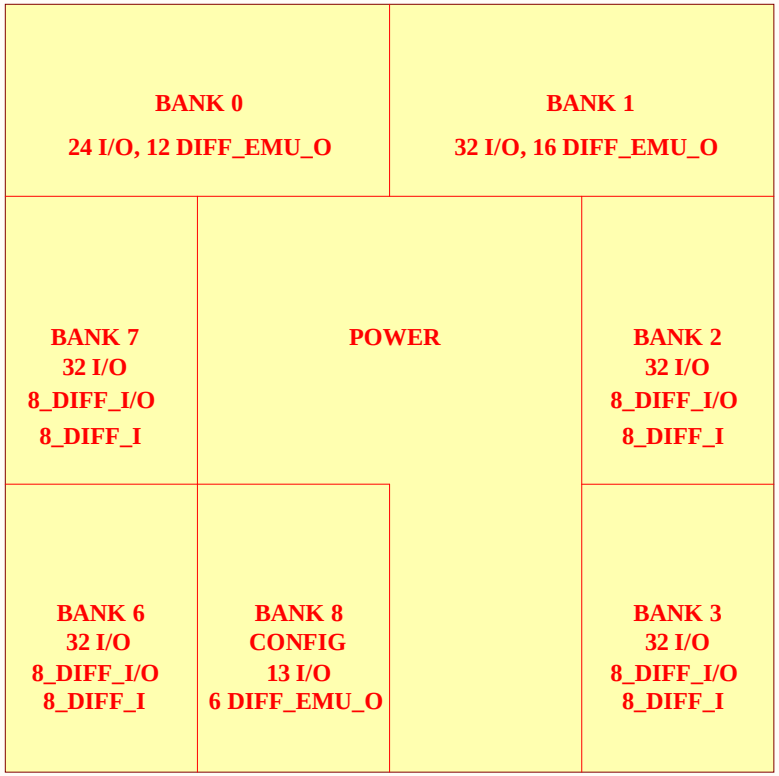
LFE5U-45F-7BG256I IO MAP



IO PLANNING:

LPDDR3 : BANK 7, BANK 6

CONFIG, LED, SWITCH : BANK 8, BANK 0

IO HEADER : BANK 1, BANK 2, BANK 3

NOTE:

I/O : Single ended I/O

DIFF_EMU_O : Differential_emulated_output

DIFF_I/O : Differential_I/O

DIFF_I : Differential_Input

Title: Block_diagram_A		Revision: V2.1
Size: A4	Project: Mimas_ECP5_Mini_V2.0.PrjPCB	
Date: 05-07-2024 Time:14:49:17	Sheet 1 of 7	
File: block_diagram_A.SchDoc		

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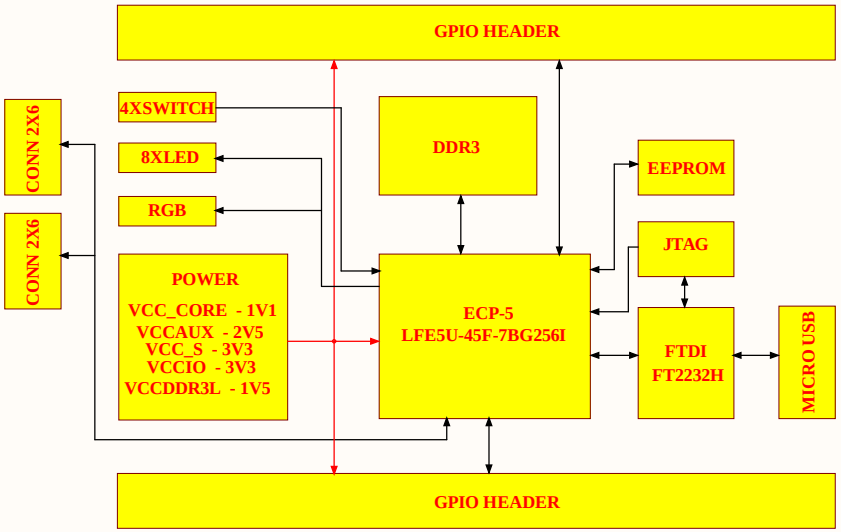
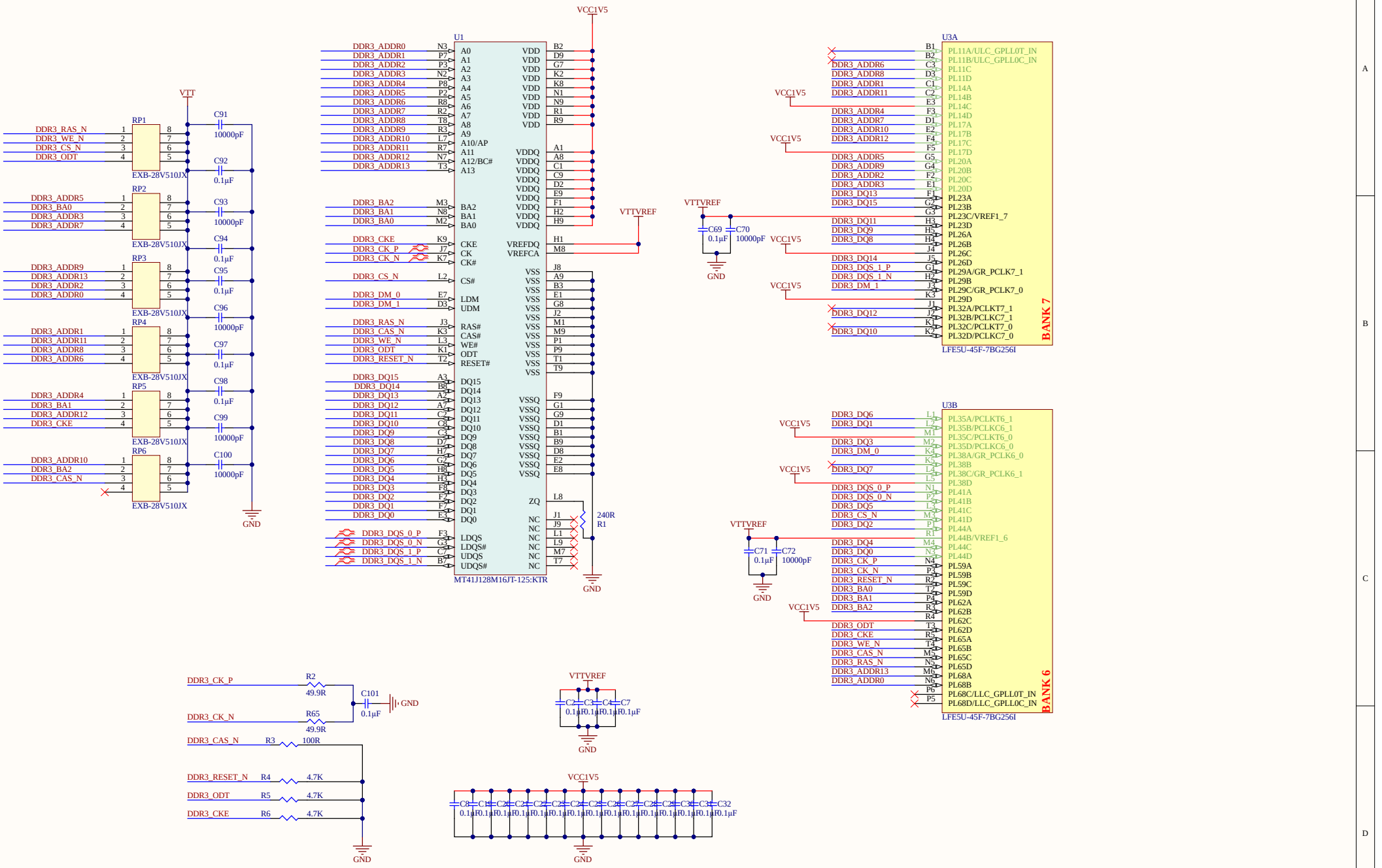
BLOCK DIAGRAM



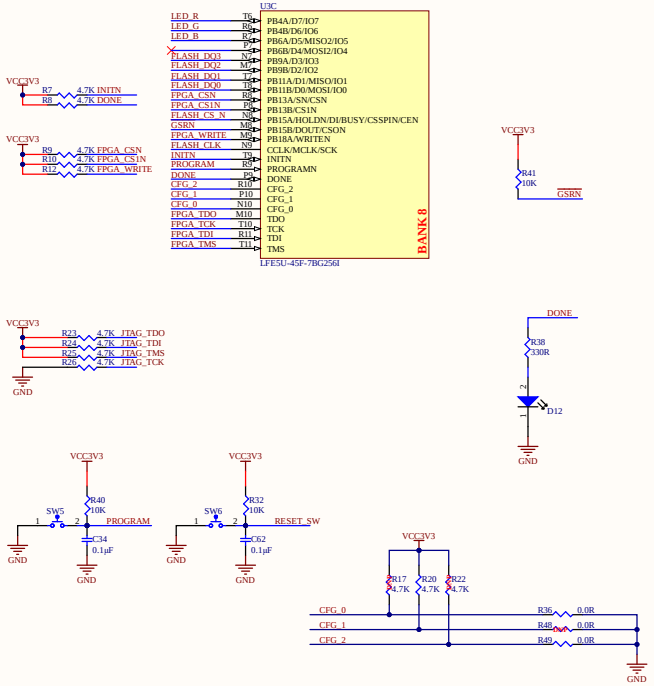
Title: Block Diagram		Revision: V2.1	Numato Lab
Size: A3	Project: Mimas_ECP5_Mini_V2.0.PrjPCB		
Date: 05-07-2024	Time: 14:49:17	Sheet 2 of 7	
File: block_diagram_B.SchDoc			

DDR3_FPGA

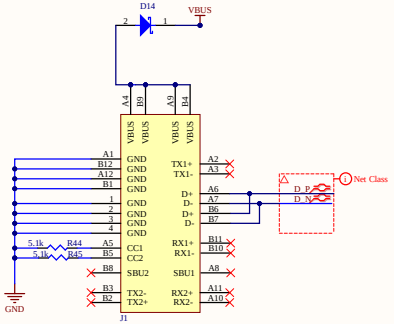


Title: DDR3L_FPGA		Revision: V2.1	Numato Lab
Size: A3	Project: Mimas_ECP5_Mini_V2.0.PrjPCB		
Date: 05-07-2024	Time: 14:49:18	Sheet 3 of 7	
File: DDR3_FPGA.SchDoc			

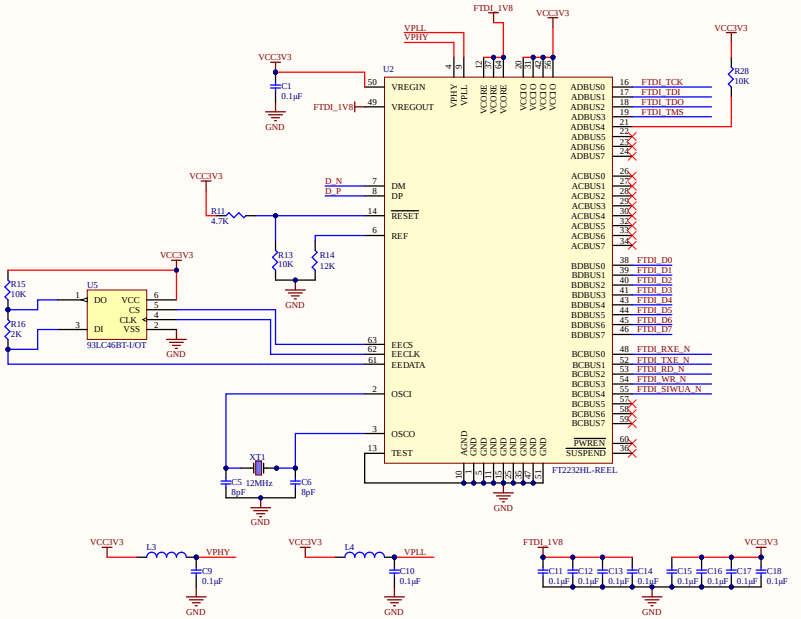
FPGA CONFIG



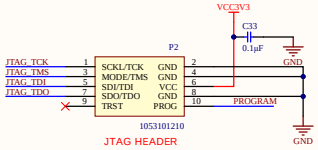
USB



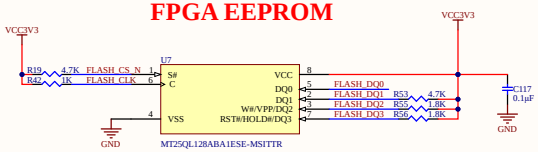
USB FTDI



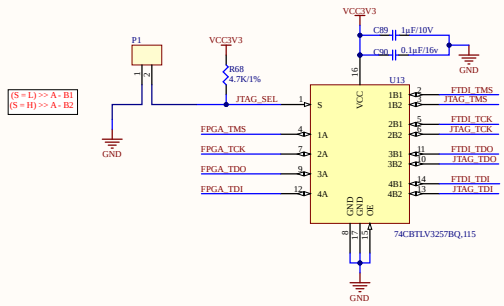
FPGA JTAG



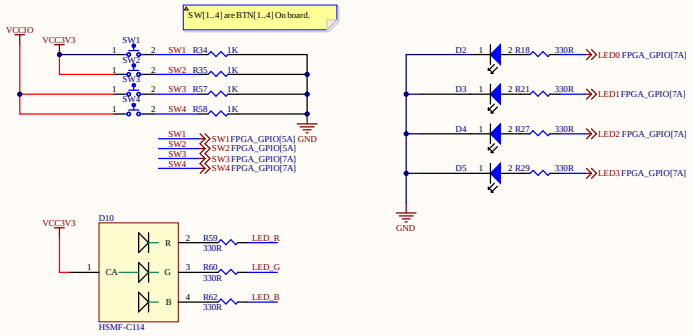
FPGA EEPROM



FPGA JTAG BUFFER

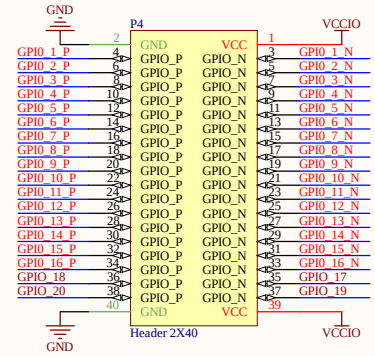


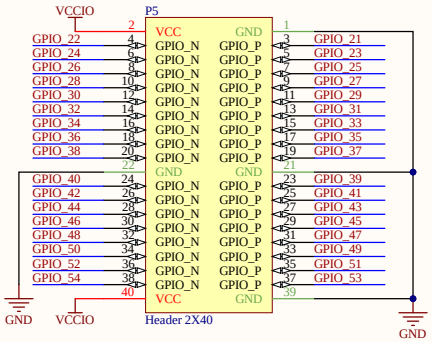
LED & SWITCHES



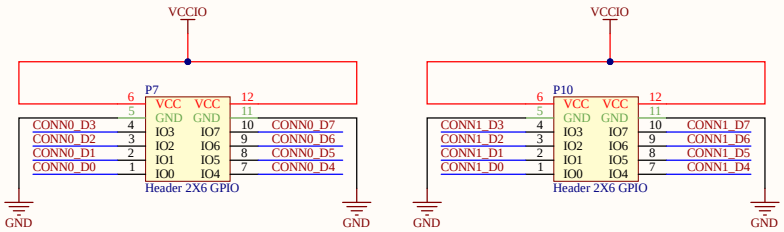
Title: FPGA_CONFIG		Revision: V2.1	Numato Lab
Size: A2	Project: Mimas_ECP5_Mini_V2.0.PrjPCB		
Date: 05-07-2024	Time: 14:49:18	Sheet 4 of 7	
File: FPGA_CONFIG.SchDoc			

CONNECTOR GPIO

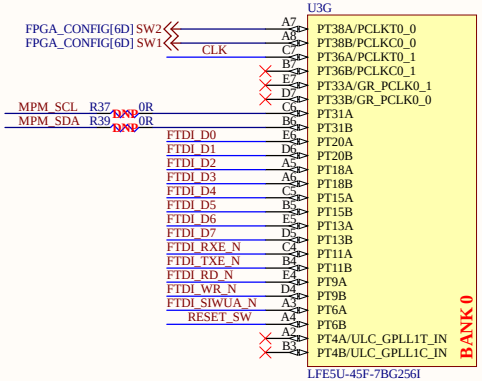


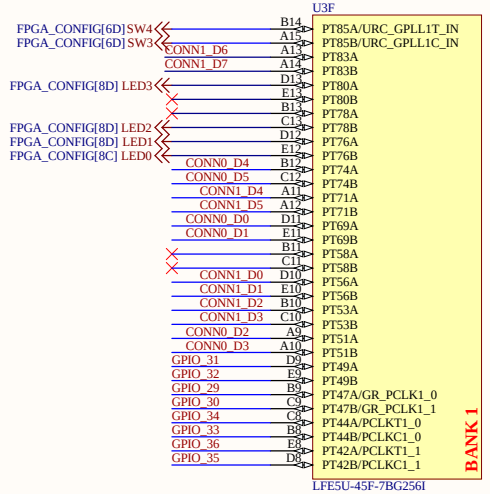


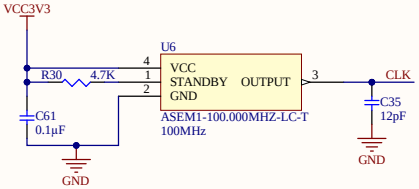
GPIO 2X6 CONNECTOR

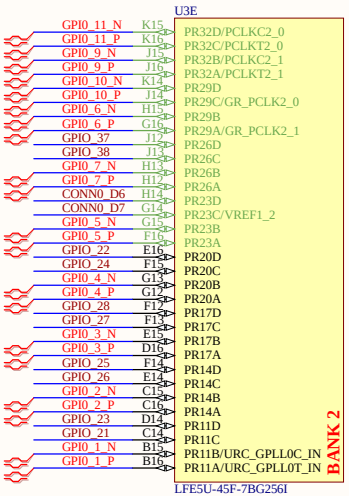


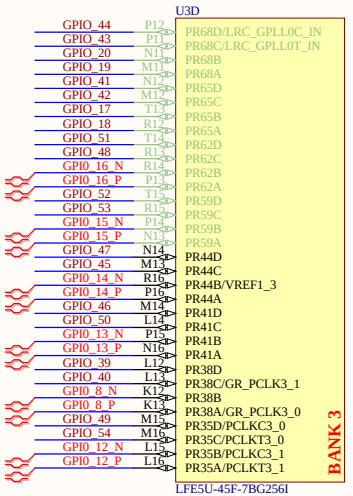
FPGA GPIO





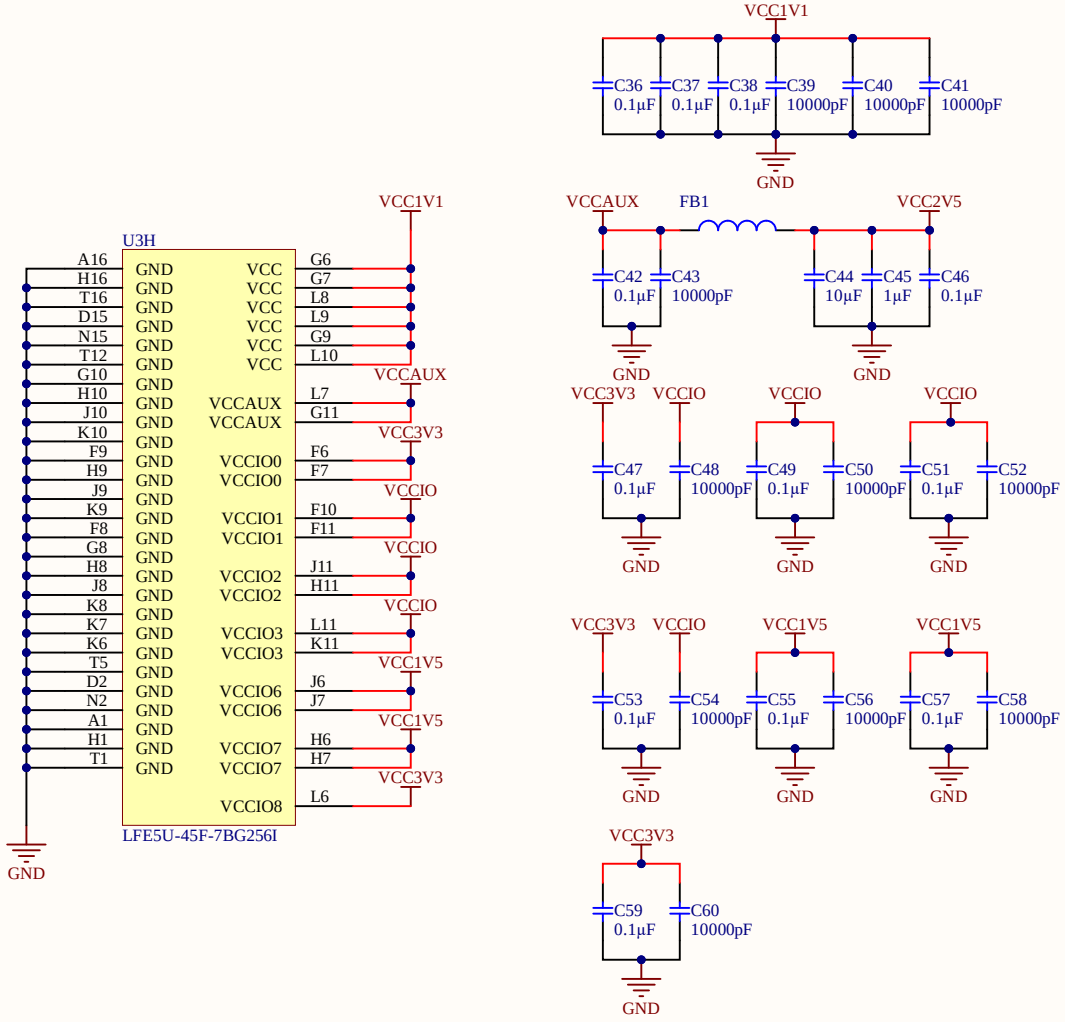






Title: FPGA_GPIO		Revision: V2.1	Numato Lab
Size: A3	Project: Mimas_ECP5_Mini_V2.0.PrjPCB		
Date: 05-07-2024	Time: 14:49:18	Sheet 5 of 7	
File: FPGA_GPIO.SchDoc			

FPGA POWER



Title: FPGA_POWER		Revision: V2.1	
Size: A4	Project: Mimas_ECP5_Mini_V2.0.PrjPCB		
Date: 05-07-2024	Time: 14:49:19	Sheet 6 of 7	
File: FPGA_POWER.SchDoc			

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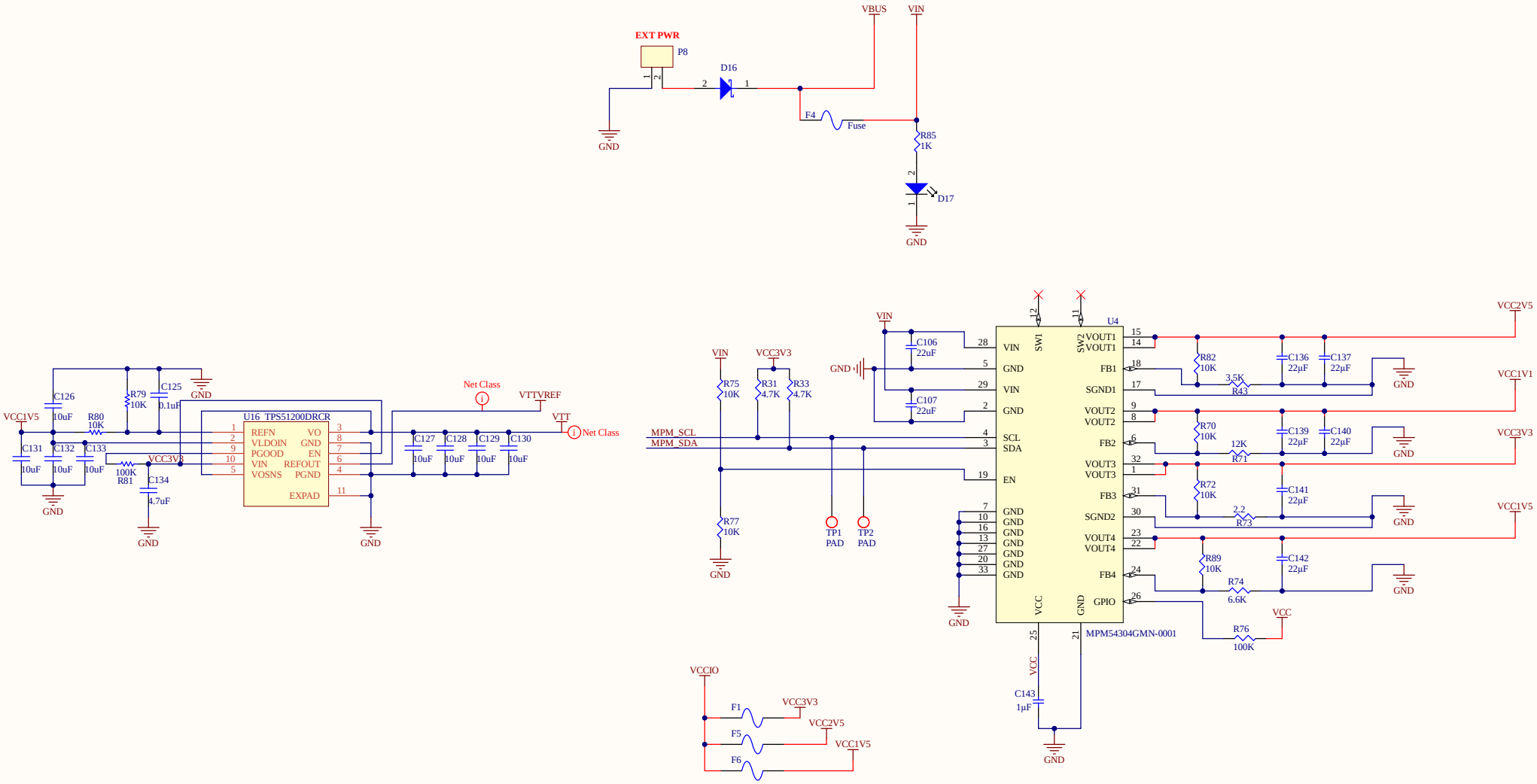
POWER SELECTOR



Title:	**Power Supply**	Revision:	V2.1
Size:	A3	Project:	Mimas_ECP5_Mini_V2.0.PrjPCB
Date:	05-07-2024	Time:	14:49:19
Sheet	7 of 7		
File:	PowerSupply.SchDoc		

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