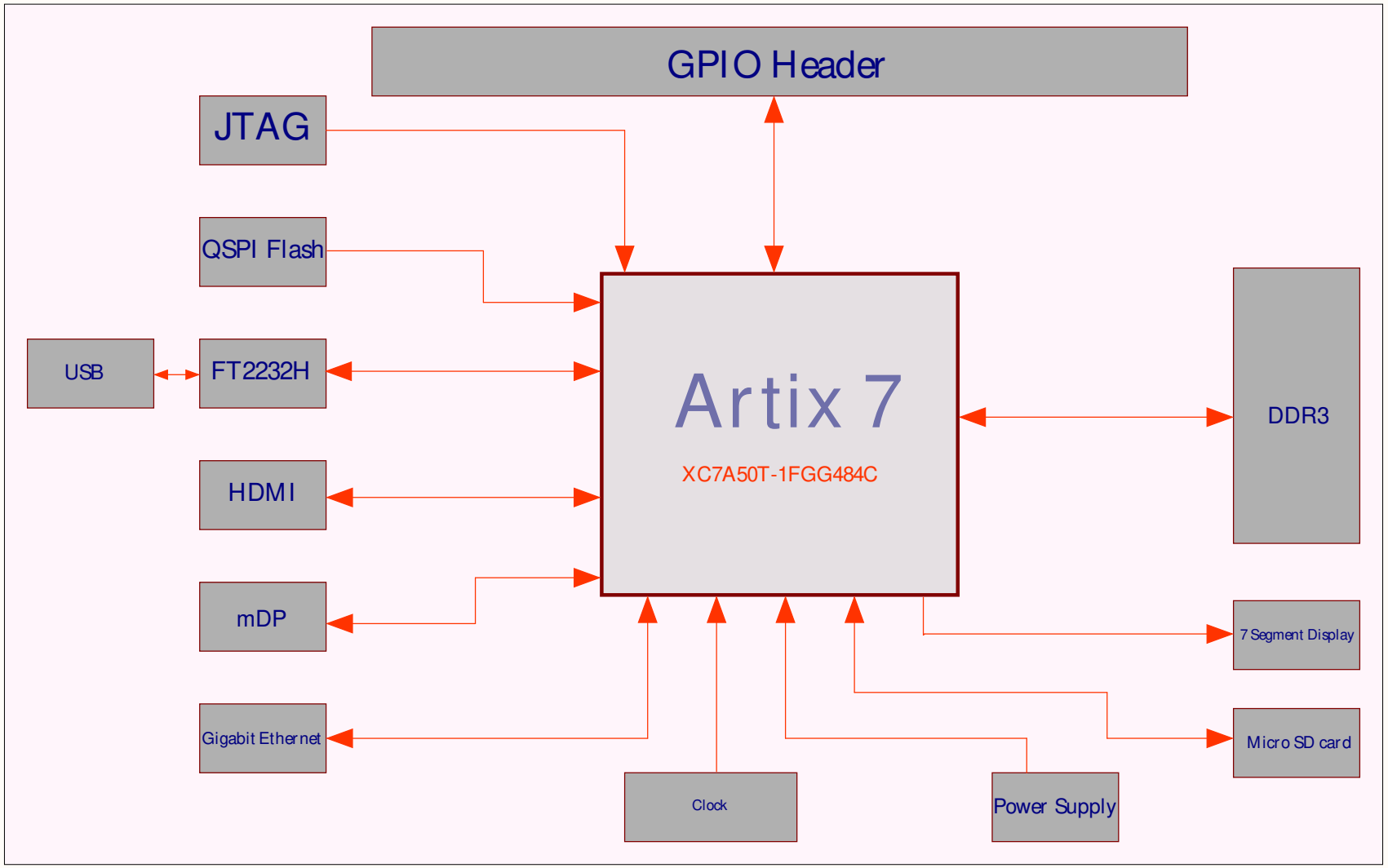
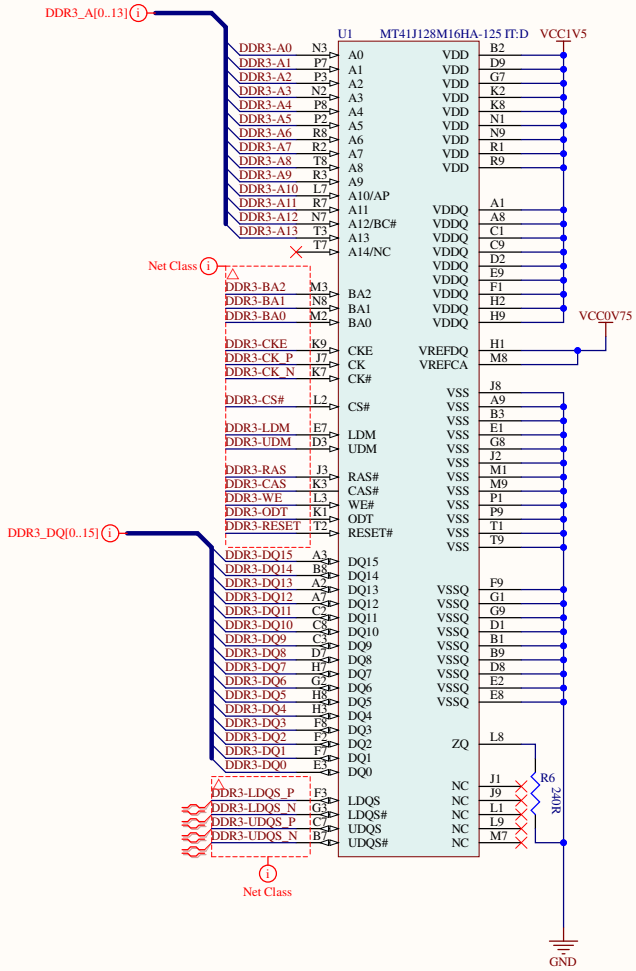
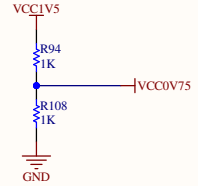
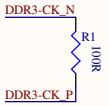


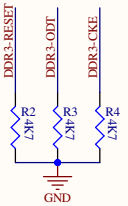
Block Diagram

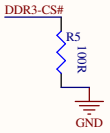
Title: MimasA7		Revision: V 3.1	Numato Systems Pvt Ltd
Size: A3	Project: MimasV3.PrjPcb		
Date: 28-07-2025	Time: 10:22:45	Sheet 1 of 13	
File: Block_Diagram.SchDoc			

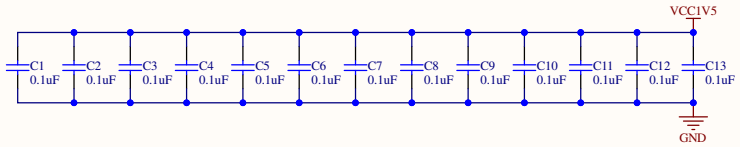


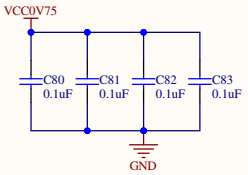






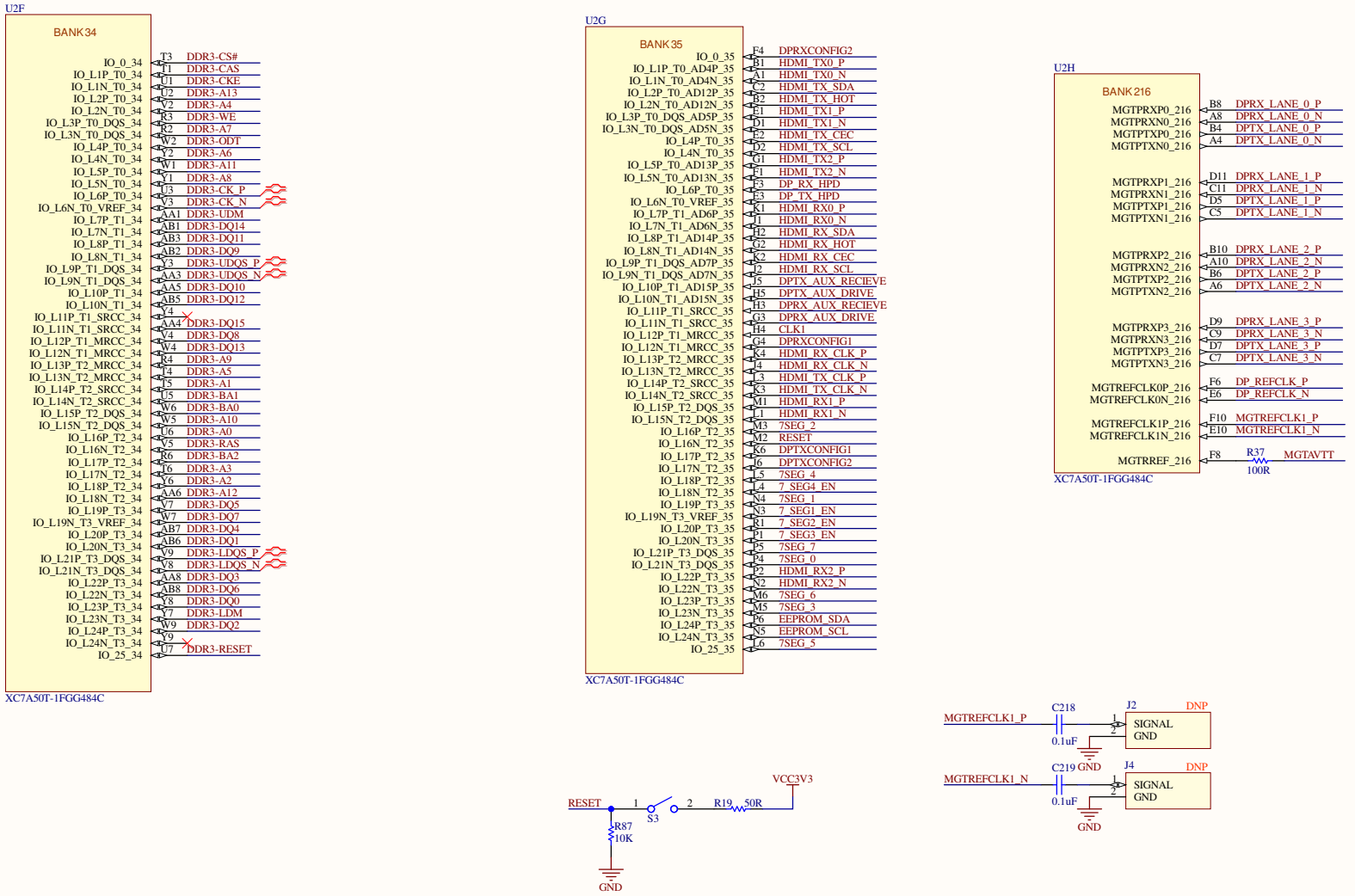






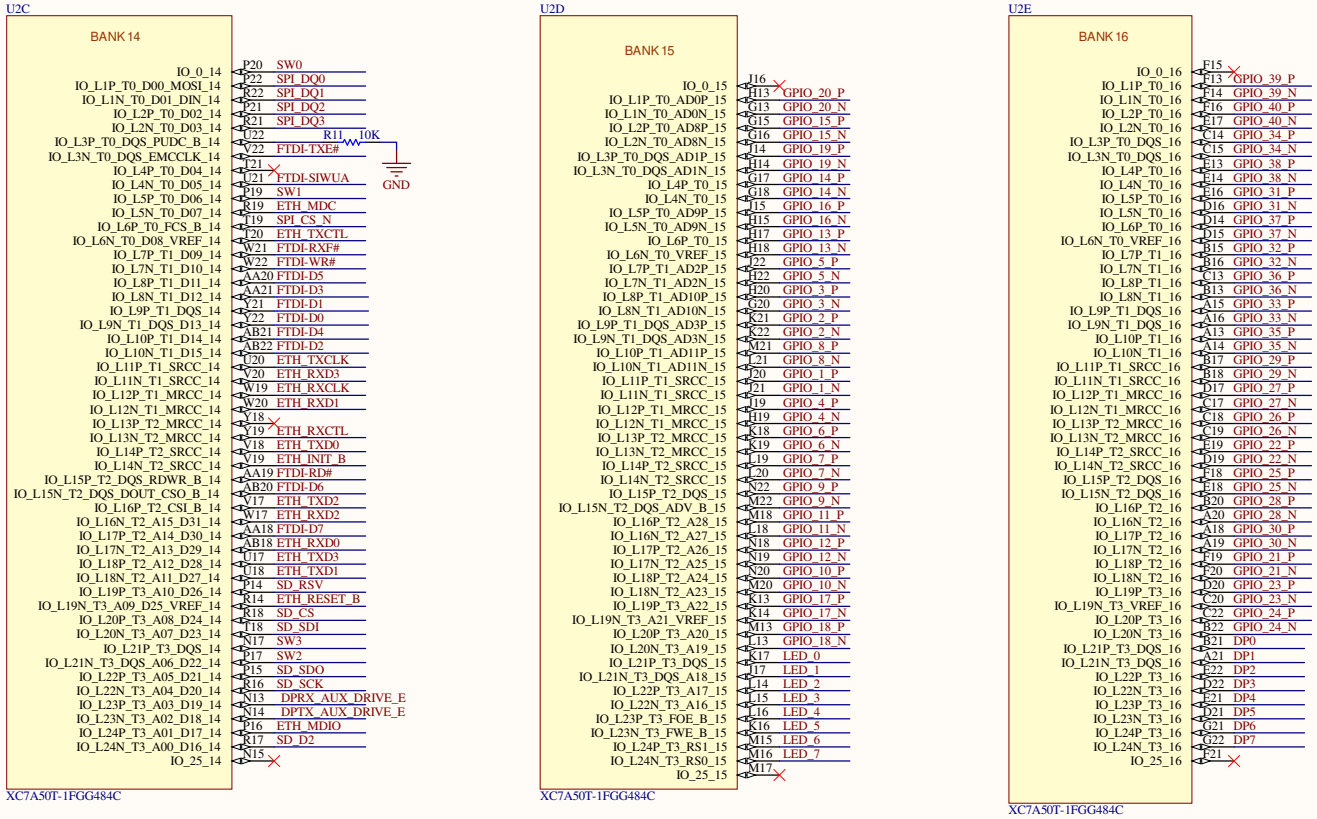
DDR3

Title: MimasA7		Revision: V 3.1	Numato Systems Pvt Ltd
Size: A3	Project: MimasV3.PrjPcb		
Date: 28-07-2025	Time: 10:22:45	Sheet 2 of 13	
File: DDR3.SchDoc			



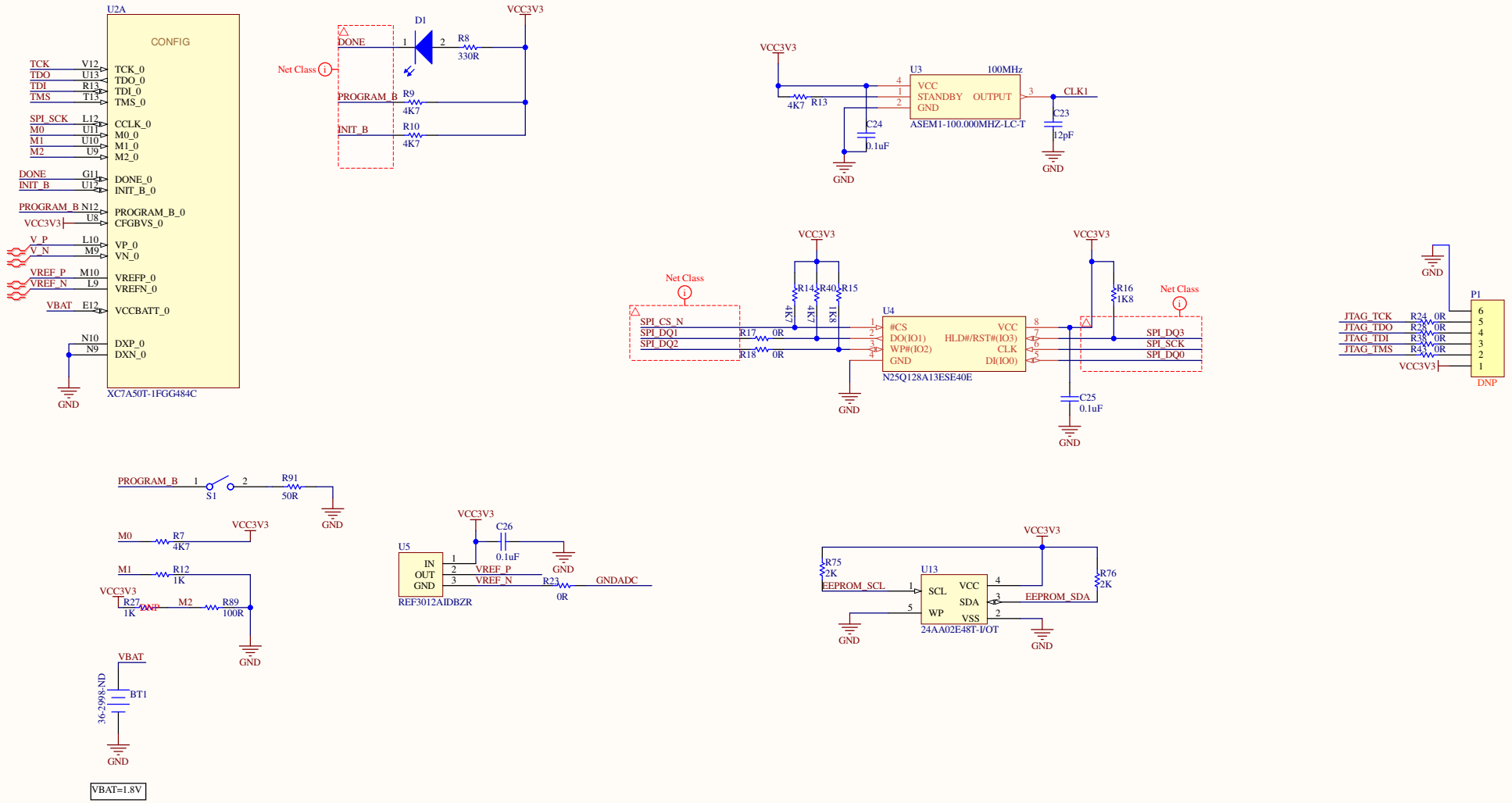
FPGA DDR3 and Mini Display Port Banks

Title: MimasA7		Revision: V 3.1	Numato Systems Pvt Ltd
Size: A3	Project: MimasV3.PrjPcb		
Date: 28-07-2025	Time: 10:22:45	Sheet 3 of 13	
File: FPGA_A.SchDoc			



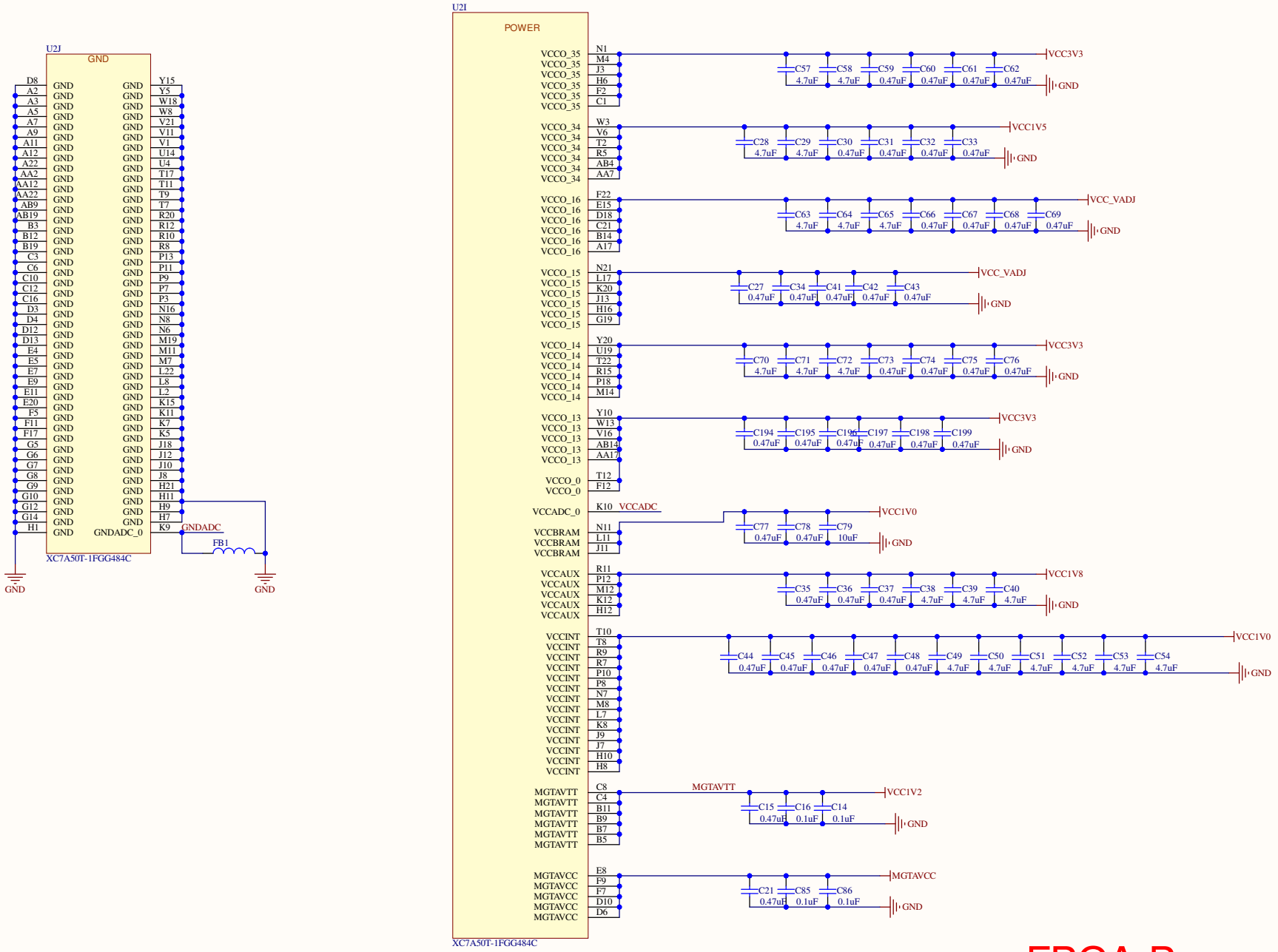
FPGA I/O,Ethernet and FTDI Banks

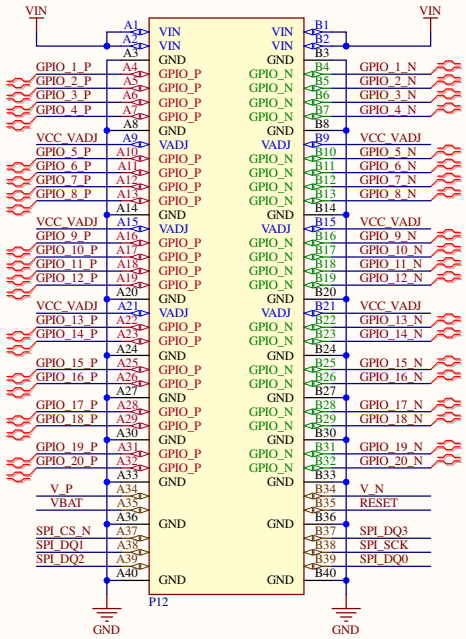
Title: MimasA7		Revision: V 3.1	Numato Systems Pvt Ltd
Size: A3	Project: MimasV3.PrjPcb		
Date: 28-07-2025	Time: 10:22:45	Sheet 4 of 13	
File: FPGA_B.SchDoc			

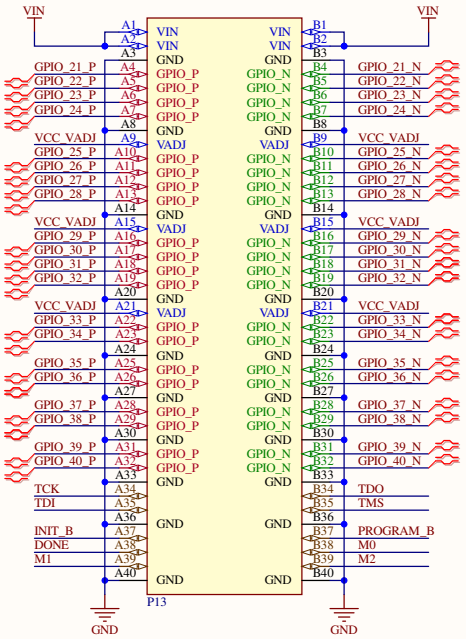


FPGA Configuration

Title: MimasA7		Revision: V 3.1	Numato Systems Pvt Ltd
Size: A3	Project: MimasV3.PrjPcb		
Date: 28-07-2025	Time: 10:22:45	Sheet 5 of 13	
File: FPGA_C.SchDoc			

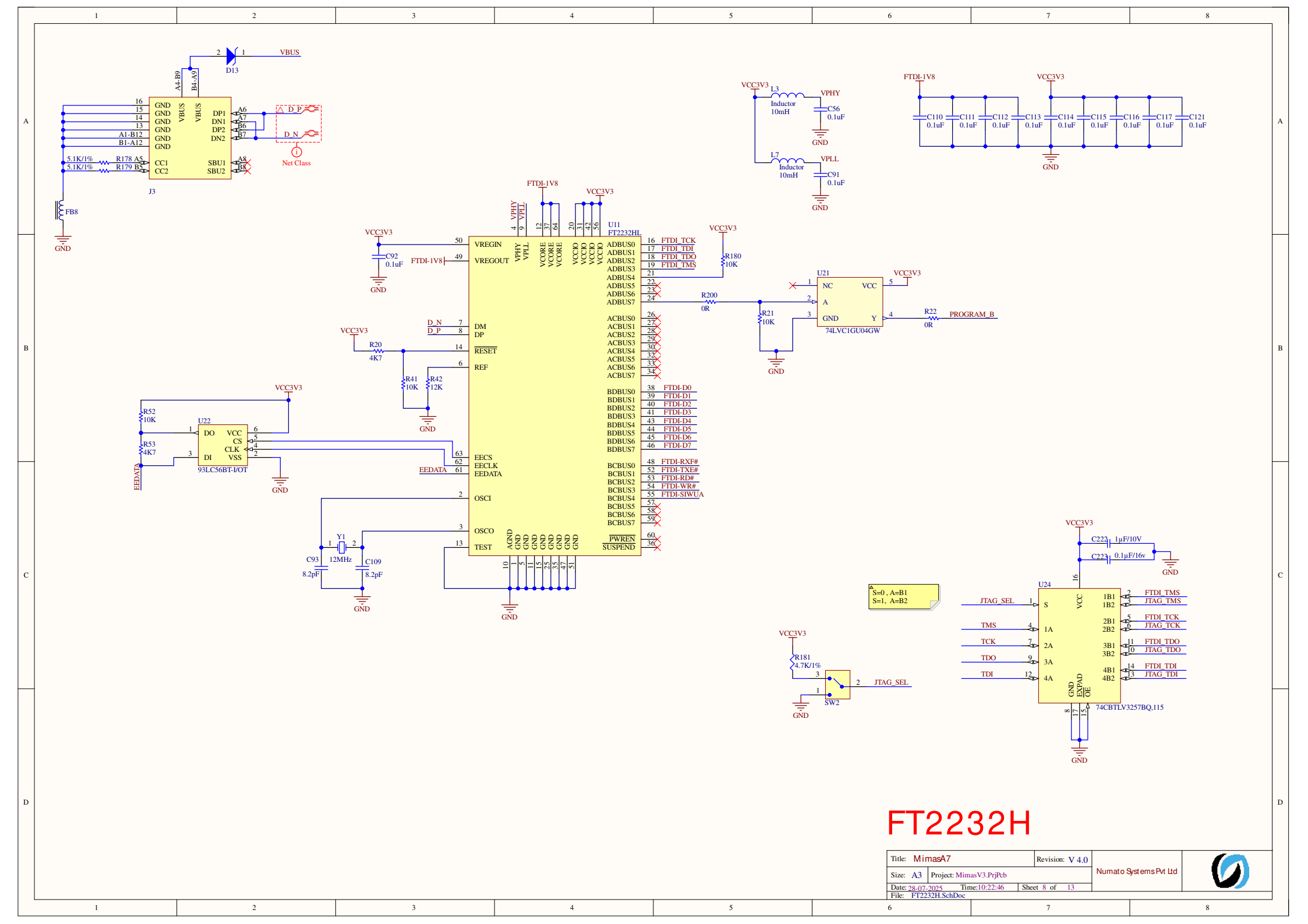

U2J
GND
XC7A50T-1FGG484C
GNDADC
FB1
U2I
POWER
XC7A50T-1FGG484C
VCC3V3
VCC1V5
VCC_VADJ
VCCADC
VCC1V0
VCC1V8
VCC1V2
MGTAVTT
MGTAVCC
GND
FPGA Power
Title: MimasA7
Revision: V 3.1
Size: A3
Project: MimasV3.PrjPcb
Numato Systems Pvt Ltd
Date: 28-07-2025
Time: 10:22:46
Sheet 6 of 13
File: FPGA_D.SchDoc

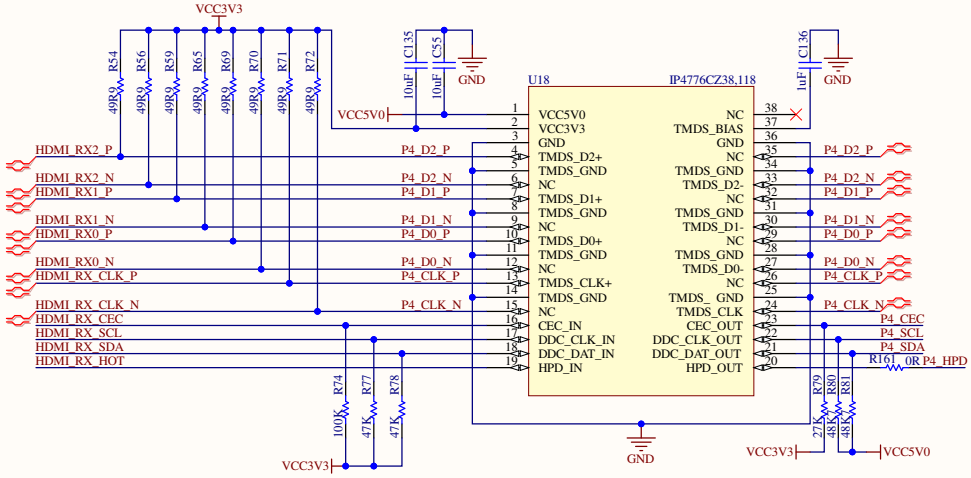




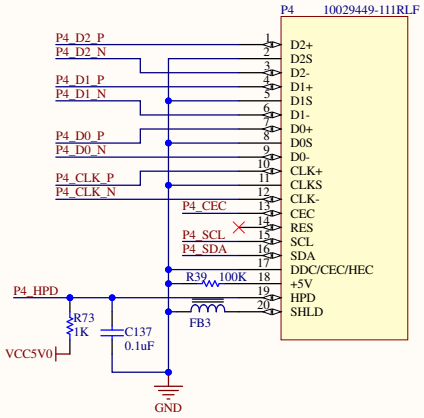
GPIO Header

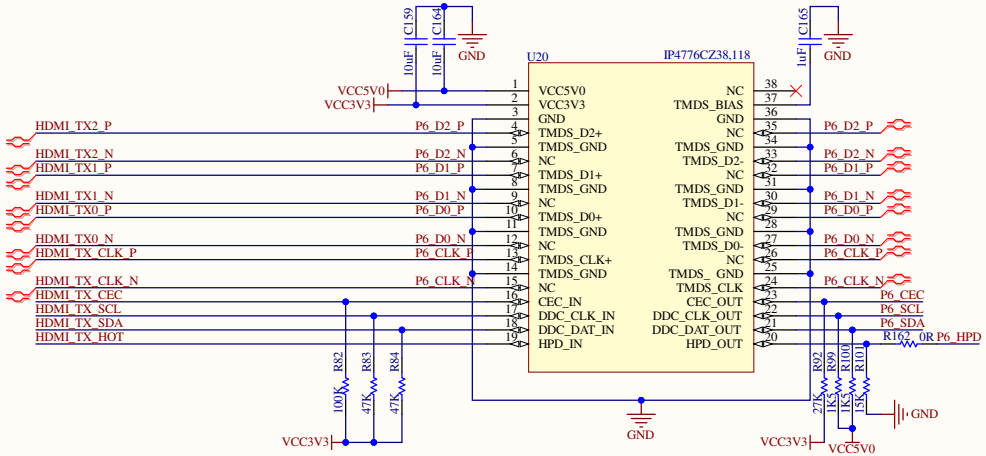
Title: MimasA7		Revision: V 3.1	Numato Systems Pvt Ltd
Size: A3	Project: MimasV3.PrjPcb		
Date: 28-07-2025	Time: 10:22:46	Sheet 7 of 13	
File: GPIO.SchDoc			


FT2232H
Title: MimasA7
Revision: V 4.0
Size: A3
Project: MimasV3.PrjPcb
Numato Systems Pvt Ltd
Date: 28-07-2025
Time: 10:22:46
Sheet 8 of 13
File: FT2232H.SchDoc
J3
U11
FT2232HL
U21
74LVC1GU04GW
U22
93LC56BT-I/OT
U24
74CBTLV3257BQ,115
D13
FB8
L3
L7
Inductor
10mH
Y1
12MHz
SW2
VBUS
D_P
D_N
Net Class
VCC3V3
FTDI-1V8
VPHY
VPLL
GND
PROGRAM_B
JTAG_SEL
TMS
TCK
TDO
TDI
EEDATA
S=0 , A=B1
S=1, A=B2

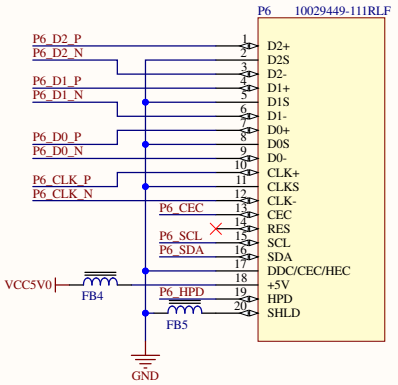


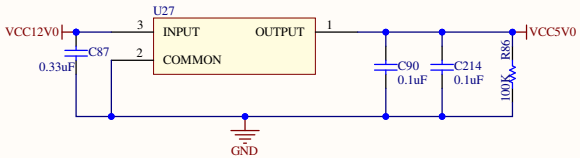
HDMI In





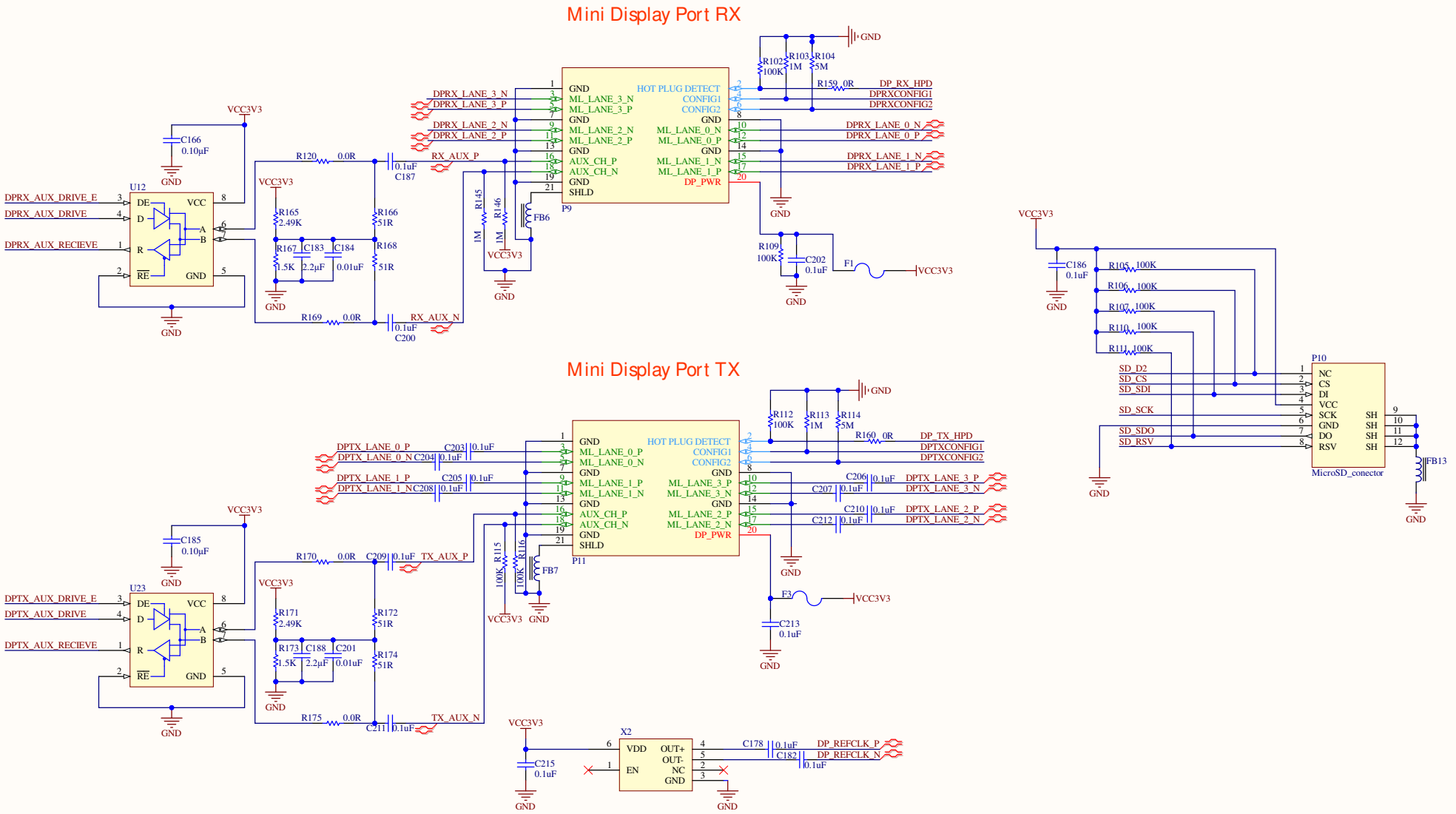
HDMI Out





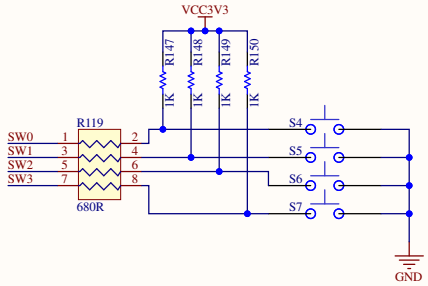
HDMI

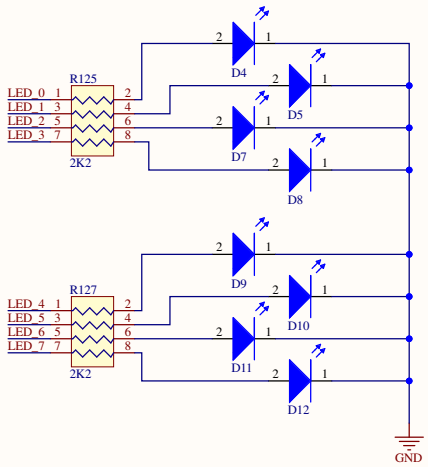
Title: MimasA7		Revision: V 3.1	Numato Systems Pvt Ltd
Size: A3	Project: MimasV3.PrjPcb		
Date: 28-07-2025	Time: 10:22:46	Sheet 9 of 13	
File: HDMI.SchDoc			

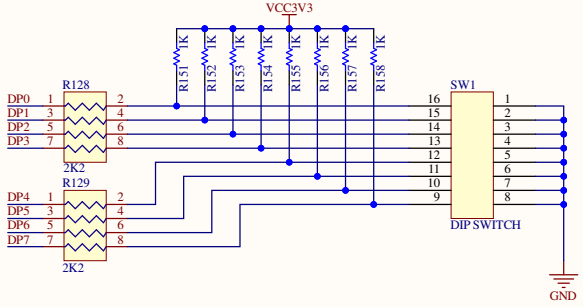


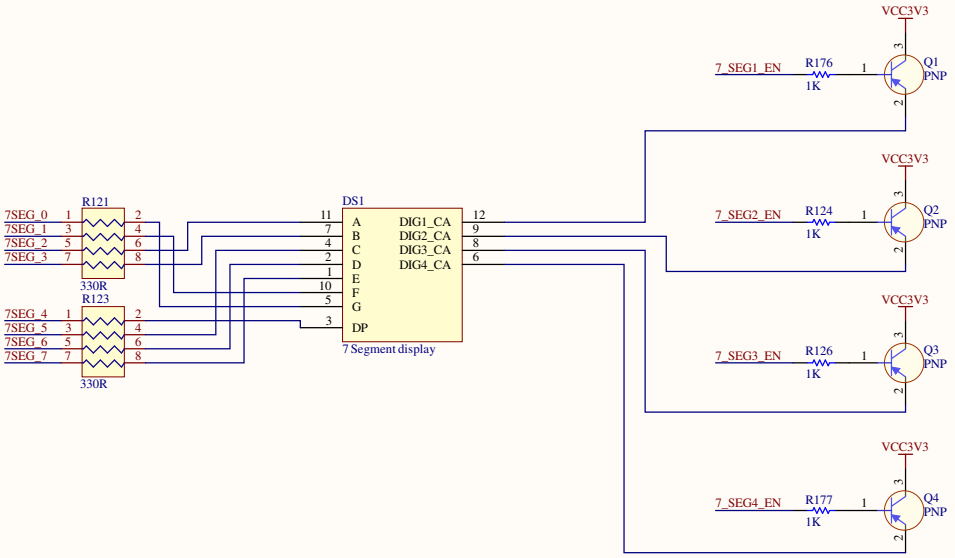
Mini Display Port & SD Card

Title: MimasA7	Revision: V 3.1	Numato Systems Pvt Ltd	
Size: A3	Project: MimasV3.PrjPcb		
Date: 28-07-2025	Time: 10:22:46	Sheet 10 of 13	
File: Display_Port.SchDoc			



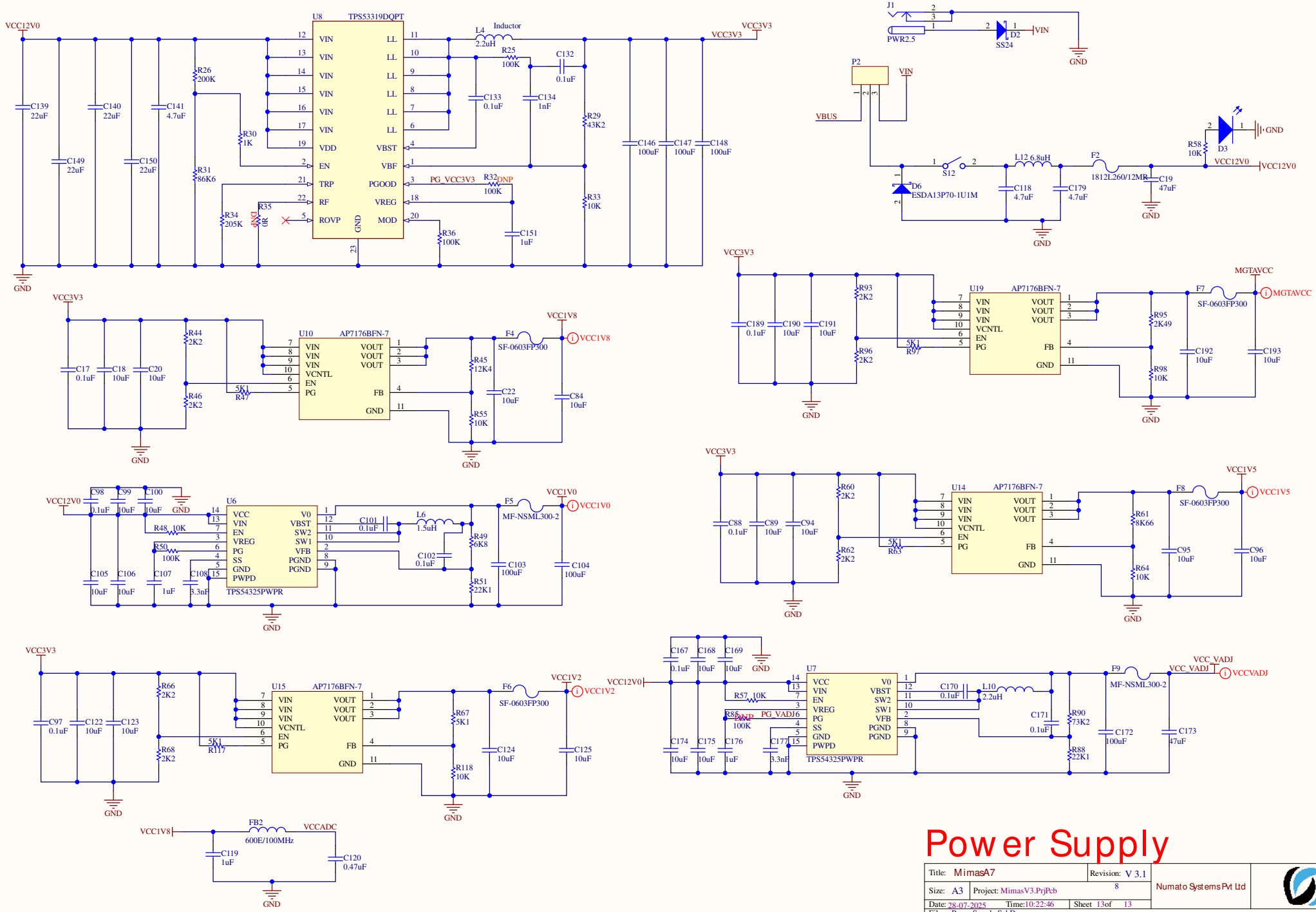






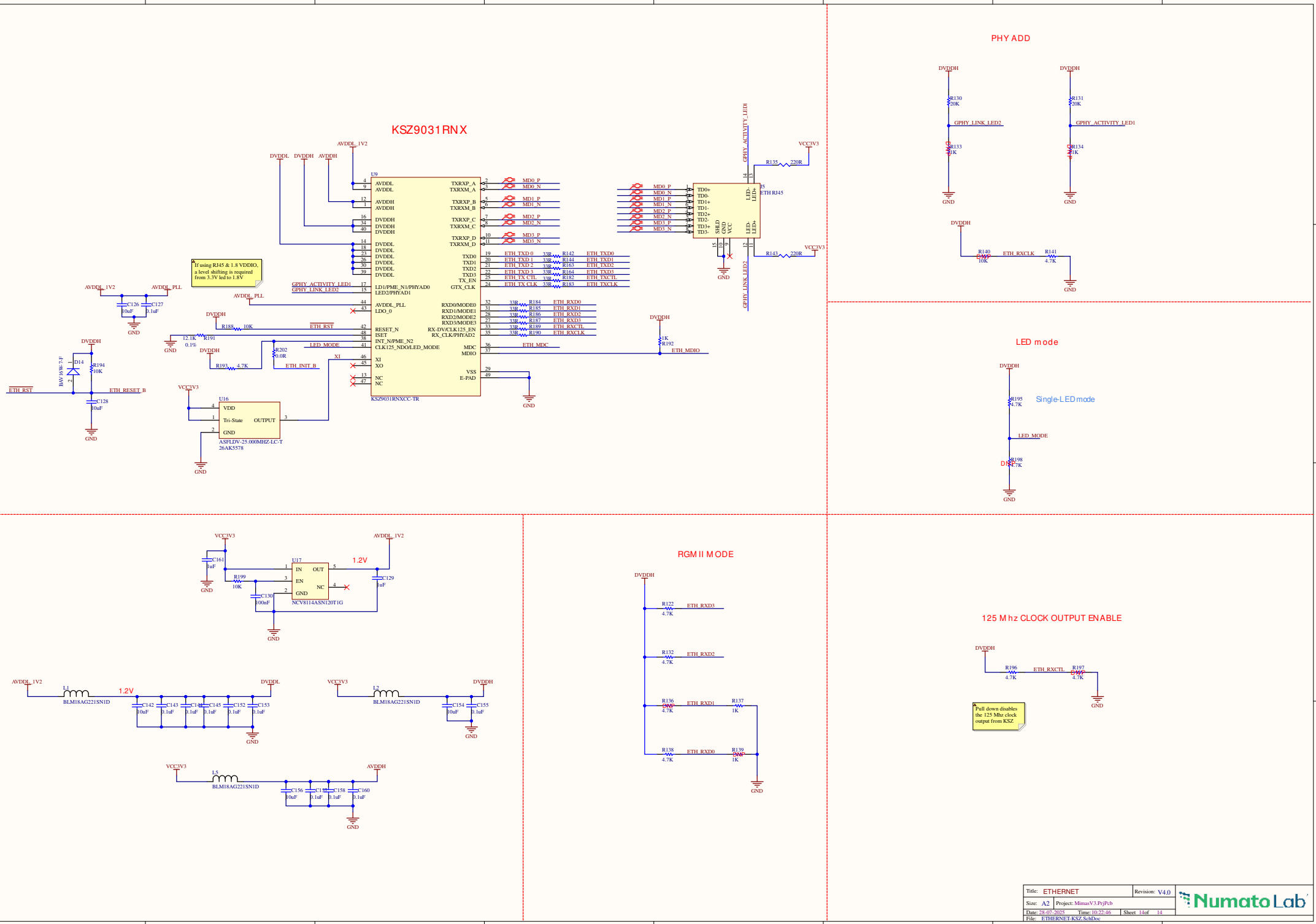
Push Button,DIP Switch,LEDs & 7 Segment Display

Title: MimasA7		Revision: V 3.1	Numato Systems Pvt Ltd
Size: A3	Project: MimasV3.PrjPcb		
Date: 28-07-2025	Time: 10:22:46	Sheet 12 of 13	
File: 7_Segment_Display.SchDoc			



Power Supply

Title: MimasA7		Revision: V 3.1	Numato Systems Pvt Ltd
Size: A3	Project: MimasV3.PrjPcb	8	
Date: 28-07-2025	Time: 10:22:46	Sheet 13 of 13	
File: PowerSupply.SchDoc			


KSZ9031RNX
KSZ9031RNXCC-TR
PHY ADD
LED mode
Single-LED mode
RGMII MODE
125 Mhz CLOCK OUTPUT ENABLE
If using RJ45 & 1.8 VDDIO, a level shifting is required from 3.3V led to 1.8V
Pull down disables the 125 Mhz clock output from KSZ
ASFLDV-25.000MHZ-LC-T
26AK5578
NCV8114ASN120T1G
BLM18AG221SN1D
ETH_RST
ETH_RESET_B
ETH_INIT_B
LED_MODE
ETH_MDC
ETH_MDIO
ETH_RXCLK
ETH_RXCTL
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_TXCTL
ETH_TXCLK
GPHY_ACTIVITY_LED1
GPHY_LINK_LED2
ETH RJ45
Title: ETHERNET
Revision: V4.0
Size: A2
Project: MimasV3.PrjPcb
Date: 28-07-2025
Time: 10:22:46
Sheet 14of 14
File: ETHERNET-KSZ.SchDoc
Numato Lab