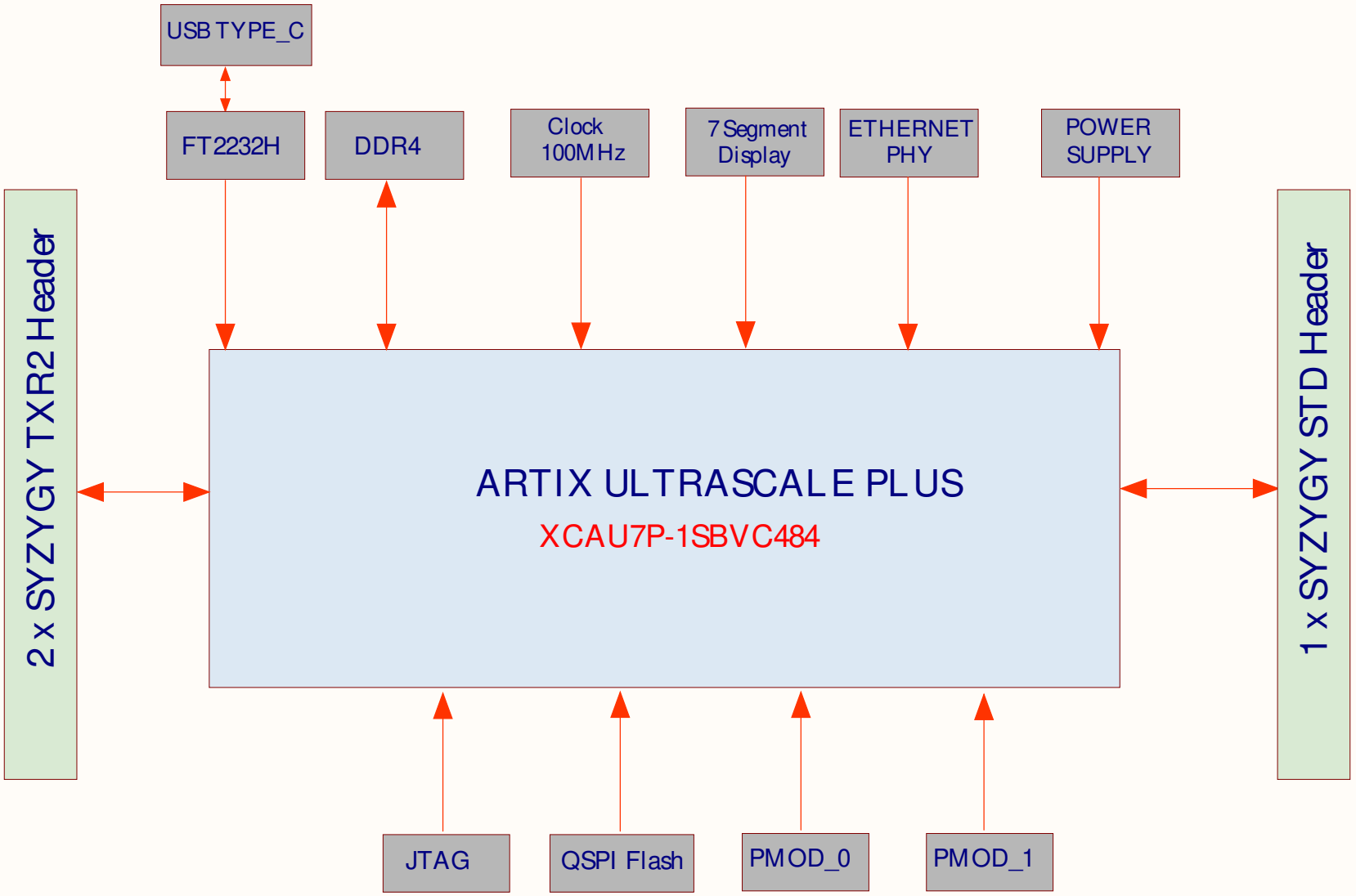
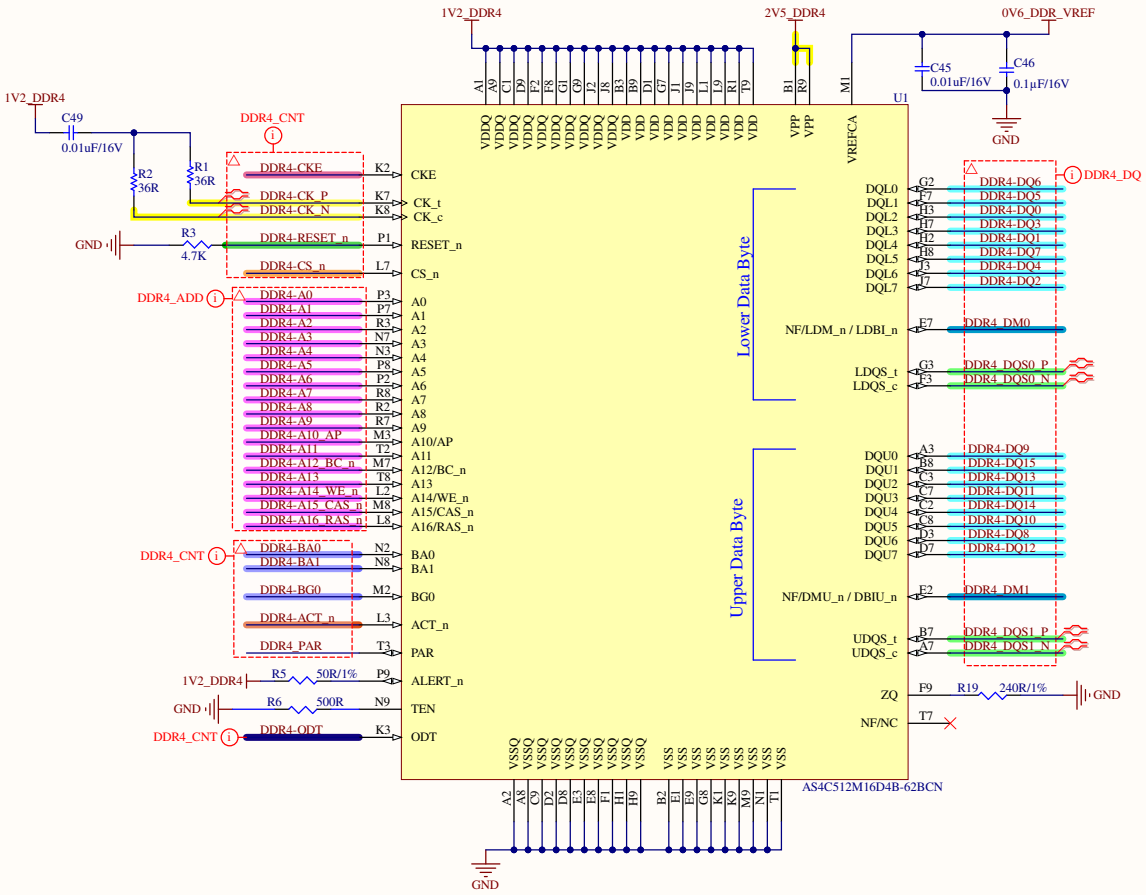


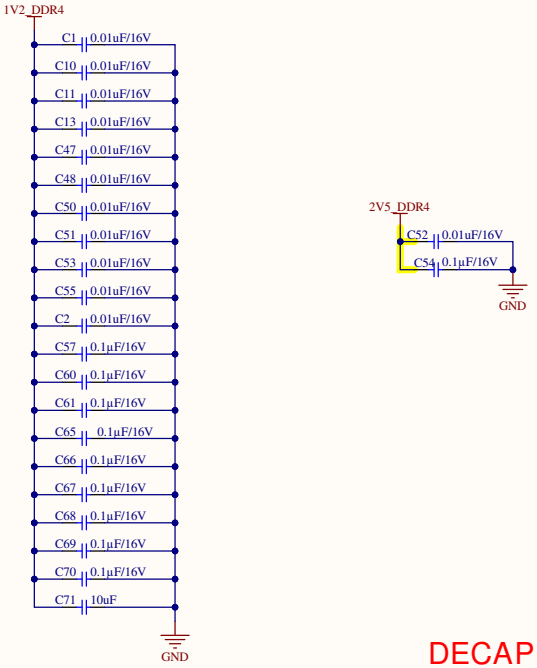
BLOCK DIAGRAM

Title: MIMASAU PLUS		Revision: A0.0
Size: A3	Project: mimas_au_plus.PrjPcb	
Date: 17-07-2025	Time: 16:31:30	Sheet 1 of 11
File: Block_Diagram.SchDoc		

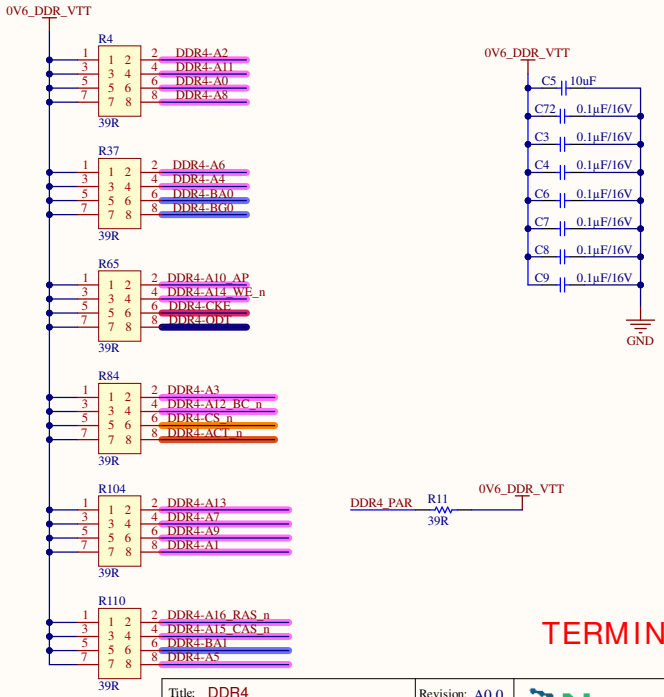
Numato Lab

DDR4

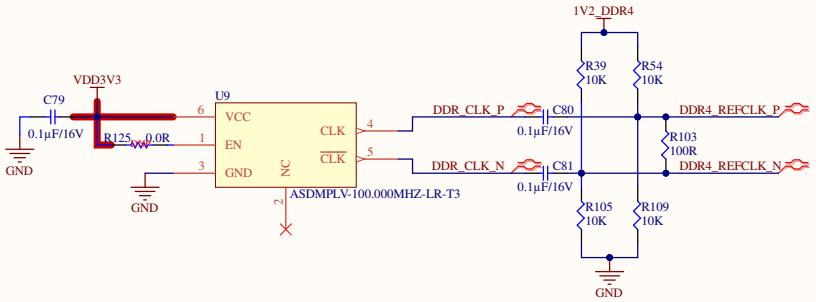




DECAP



TERMINATION

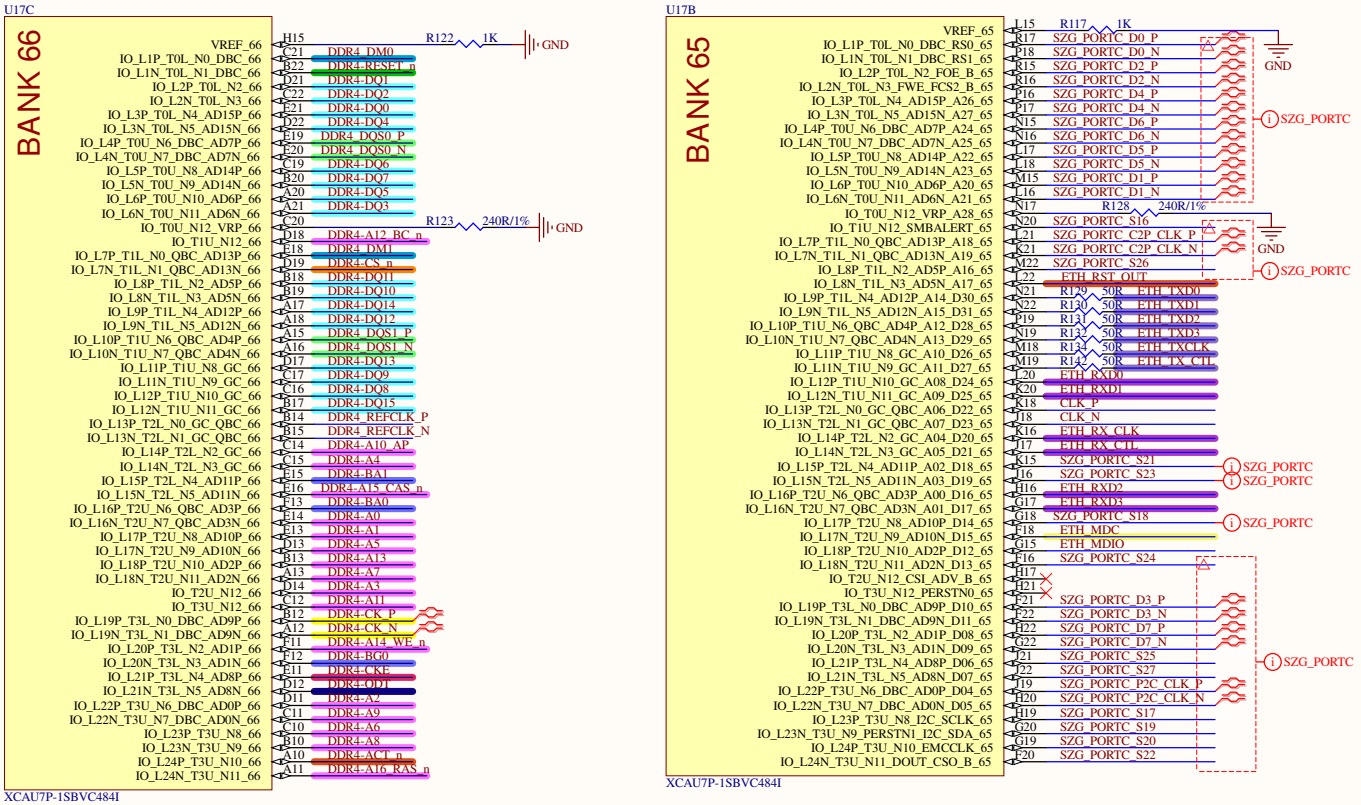


DDR REFERENCE CLOCK 100MHz

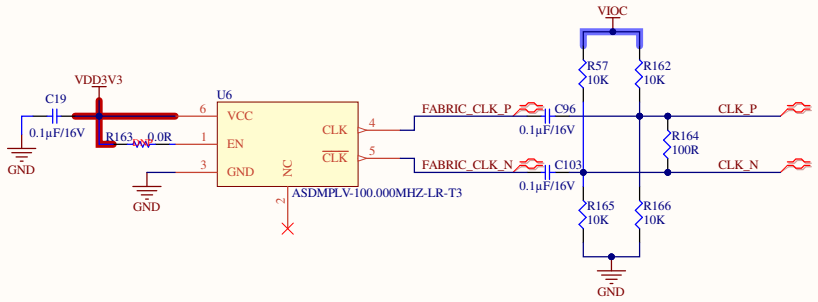
Title: DDR4		Revision: A0.0	
Size: A3	Project: mimas_au_plus.PrjPcb		
Date: 17-07-2025	Time: 16:31:30	Sheet 2 of 11	
File: DDR4.SchDoc			

Numato Lab

HP BANKS

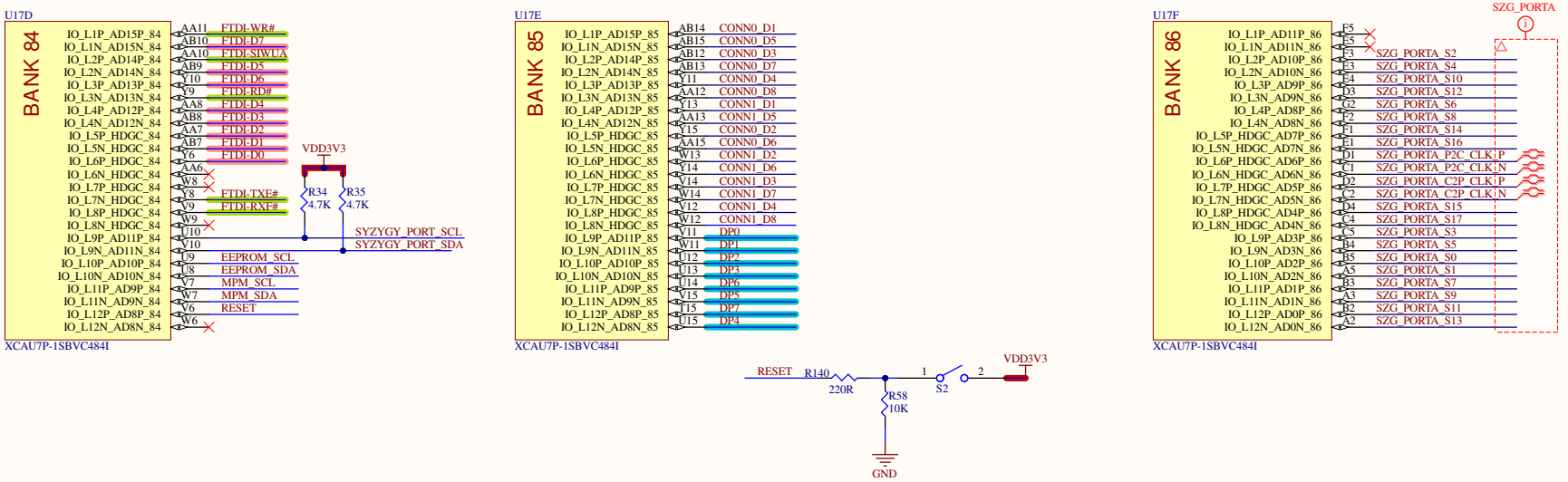


FABRIC CLOCK 100MHz

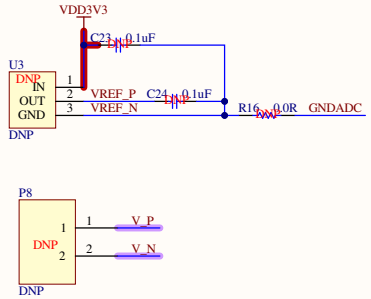


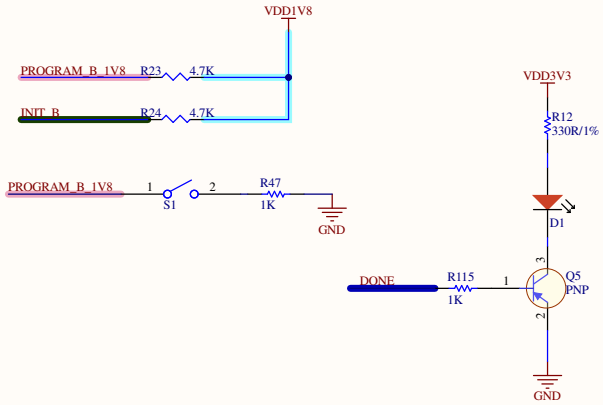
Title: FPGA_A		Revision: A0.0	Numato Lab
Size: A3	Project: mimas_au_plus.PrjPcb		
Date: 17-07-2025	Time: 16:31:31	Sheet 3 of 11	
File: FPGA_A.SchDoc			

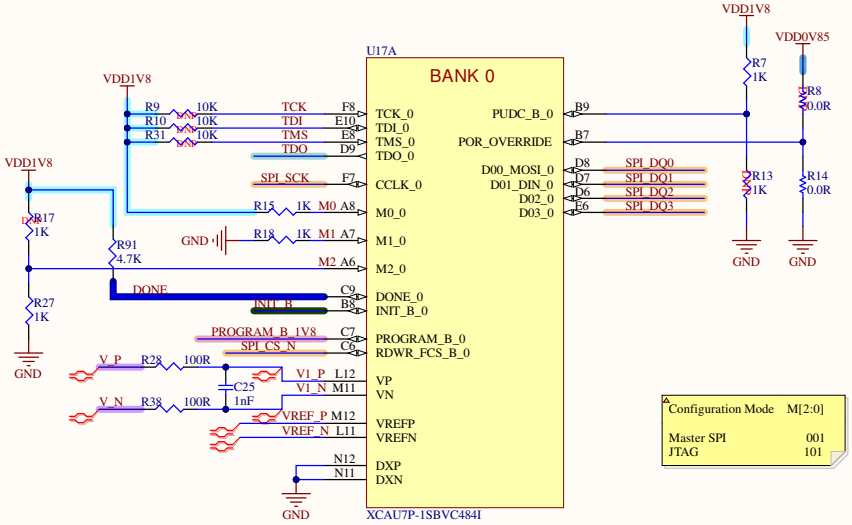
HD BANKS



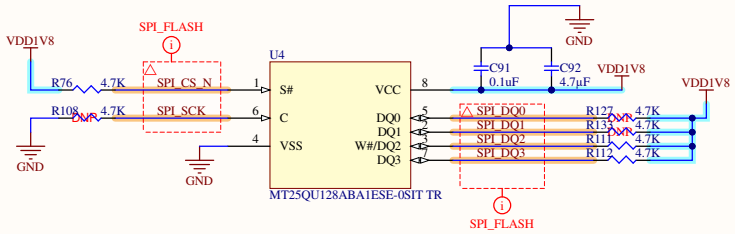
Title: FPGA_B		Revision: A0.0	Numato Lab
Size: A3	Project: mimas_au_plus.PrjPcb		
Date: 17-07-2025	Time: 16:31:32	Sheet 4 of 11	
File: FPGA_B.SchDoc			



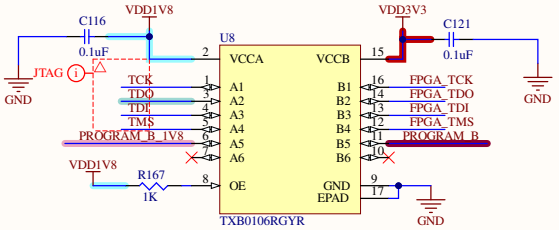


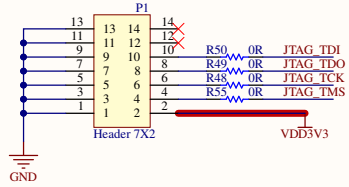


SPI FLASH

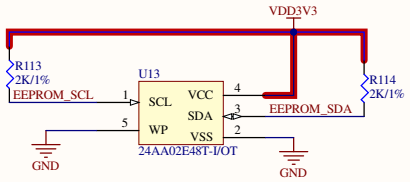


JTAG



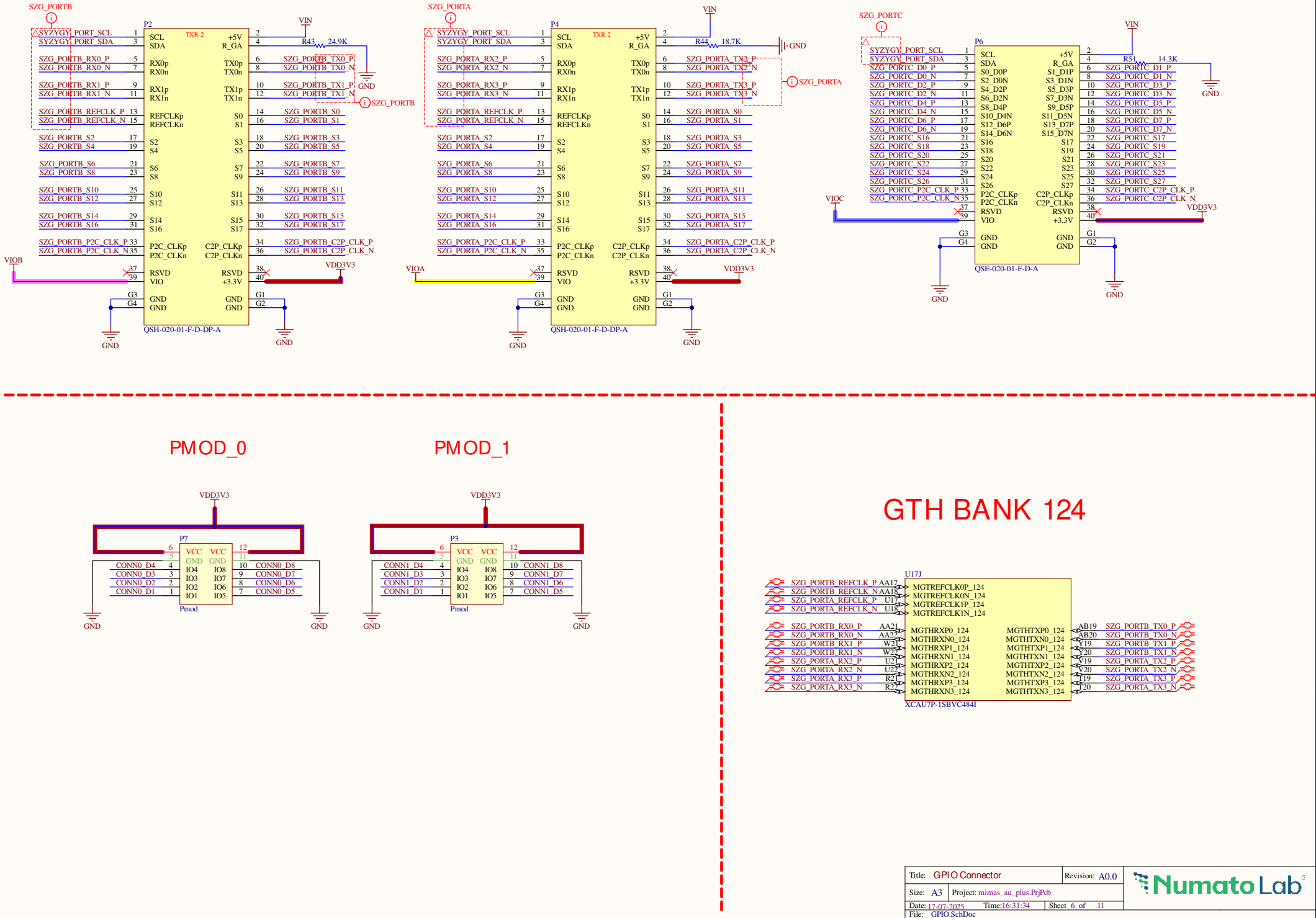


EEPROM

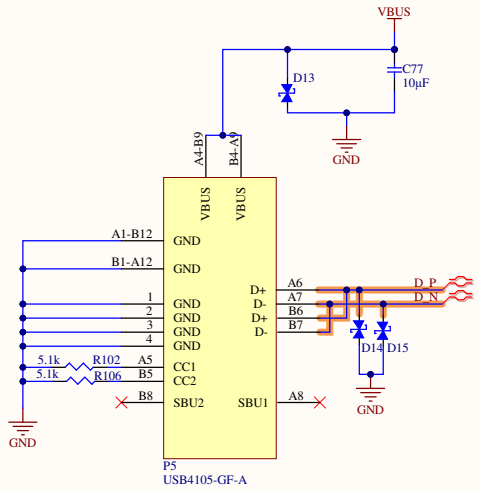


FPGA Configuration

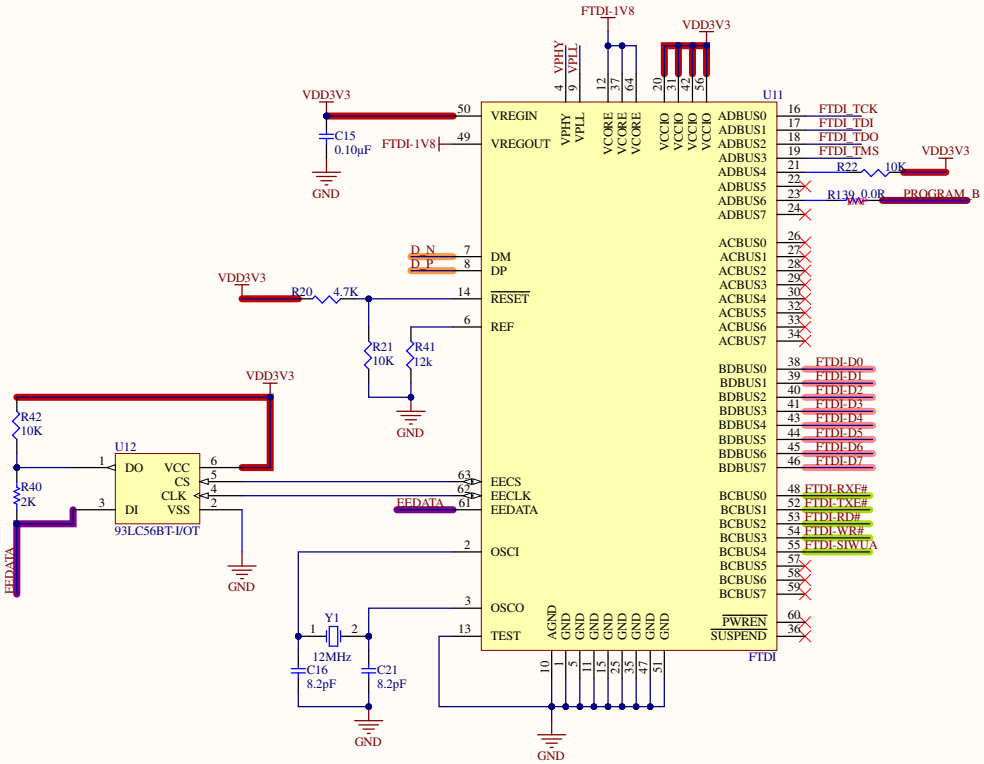
Title: FPGA_C		Revision: A0.0	Numato Lab
Size: A3	Project: mimas_au_plus.PrjPcb		
Date: 17-07-2025	Time: 16:31:33	Sheet 5 of 11	
File: FPGA_C.SchDoc			

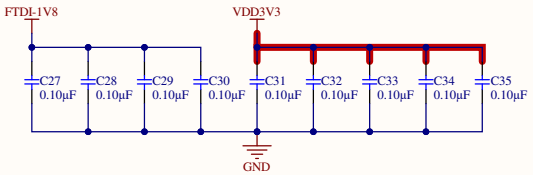

SZG_PORTB
P2
TXR-2
SYZYGY_PORT_SCL
SYZYGY_PORT_SDA
SCL
SDA
+5V
R_GA
R43
24.9K
VIN
SZG_PORTB_RX0_P
SZG_PORTB_RX0_N
RX0p
RX0n
TX0p
TX0n
SZG_PORTB_TX0_P
SZG_PORTB_TX0_N
SZG_PORTB_RX1_P
SZG_PORTB_RX1_N
RX1p
RX1n
TX1p
TX1n
SZG_PORTB_TX1_P
SZG_PORTB_TX1_N
GND
SZG_PORTB
SZG_PORTB_REFCLK_P
SZG_PORTB_REFCLK_N
REFCLKp
REFCLKn
S0
S1
SZG_PORTB_S0
SZG_PORTB_S1
SZG_PORTB_S2
SZG_PORTB_S4
S2
S4
S3
S5
SZG_PORTB_S3
SZG_PORTB_S5
SZG_PORTB_S6
SZG_PORTB_S8
S6
S8
S7
S9
SZG_PORTB_S7
SZG_PORTB_S9
SZG_PORTB_S10
SZG_PORTB_S12
S10
S12
S11
S13
SZG_PORTB_S11
SZG_PORTB_S13
SZG_PORTB_S14
SZG_PORTB_S16
S14
S16
S15
S17
SZG_PORTB_S15
SZG_PORTB_S17
SZG_PORTB_P2C_CLK_P
SZG_PORTB_P2C_CLK_N
P2C_CLKp
P2C_CLKn
C2P_CLKp
C2P_CLKn
SZG_PORTB_C2P_CLK_P
SZG_PORTB_C2P_CLK_N
VIOB
RSVD
VIO
+3.3V
VDD3V3
GND
G1
G2
G3
G4
QSH-020-01-F-D-DP-A
SZG_PORTA
P4
R44
18.7K
SZG_PORTA_RX2_P
SZG_PORTA_RX2_N
SZG_PORTA_TX2_P
SZG_PORTA_TX2_N
SZG_PORTA_RX3_P
SZG_PORTA_RX3_N
SZG_PORTA_TX3_P
SZG_PORTA_TX3_N
SZG_PORTA_REFCLK_P
SZG_PORTA_REFCLK_N
SZG_PORTA_S0
SZG_PORTA_S1
SZG_PORTA_S2
SZG_PORTA_S4
SZG_PORTA_S3
SZG_PORTA_S5
SZG_PORTA_S6
SZG_PORTA_S8
SZG_PORTA_S7
SZG_PORTA_S9
SZG_PORTA_S10
SZG_PORTA_S12
SZG_PORTA_S11
SZG_PORTA_S13
SZG_PORTA_S14
SZG_PORTA_S16
SZG_PORTA_S15
SZG_PORTA_S17
SZG_PORTA_P2C_CLK_P
SZG_PORTA_P2C_CLK_N
SZG_PORTA_C2P_CLK_P
SZG_PORTA_C2P_CLK_N
VIOA
SZG_PORTC
P6
R51
14.3K
SZG_PORTC_D0_P
SZG_PORTC_D0_N
SZG_PORTC_D1_P
SZG_PORTC_D1_N
SZG_PORTC_D2_P
SZG_PORTC_D2_N
SZG_PORTC_D3_P
SZG_PORTC_D3_N
SZG_PORTC_D4_P
SZG_PORTC_D4_N
SZG_PORTC_D5_P
SZG_PORTC_D5_N
SZG_PORTC_D6_P
SZG_PORTC_D6_N
SZG_PORTC_D7_P
SZG_PORTC_D7_N
SZG_PORTC_S16
SZG_PORTC_S18
SZG_PORTC_S20
SZG_PORTC_S22
SZG_PORTC_S24
SZG_PORTC_S26
SZG_PORTC_S17
SZG_PORTC_S19
SZG_PORTC_S21
SZG_PORTC_S23
SZG_PORTC_S25
SZG_PORTC_S27
SZG_PORTC_P2C_CLK_P
SZG_PORTC_P2C_CLK_N
SZG_PORTC_C2P_CLK_P
SZG_PORTC_C2P_CLK_N
VIOC
QSE-020-01-F-D-A
PMOD_0
PMOD_1
P7
P3
VCC
GND
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
CONN0_D1
CONN0_D2
CONN0_D3
CONN0_D4
CONN0_D5
CONN0_D6
CONN0_D7
CONN0_D8
CONN1_D1
CONN1_D2
CONN1_D3
CONN1_D4
CONN1_D5
CONN1_D6
CONN1_D7
CONN1_D8
Pmod
GTH BANK 124
U17J
SZG_PORTB_REFCLK_P
SZG_PORTB_REFCLK_N
SZG_PORTA_REFCLK_P
SZG_PORTA_REFCLK_N
MGTREFCLK0P_124
MGTREFCLK0N_124
MGTREFCLK1P_124
MGTREFCLK1N_124
SZG_PORTB_RX0_P
SZG_PORTB_RX0_N
SZG_PORTB_RX1_P
SZG_PORTB_RX1_N
SZG_PORTA_RX2_P
SZG_PORTA_RX2_N
SZG_PORTA_RX3_P
SZG_PORTA_RX3_N
MGTHRXP0_124
MGTHRXN0_124
MGTHRXP1_124
MGTHRXN1_124
MGTHRXP2_124
MGTHRXN2_124
MGTHRXP3_124
MGTHRXN3_124
MGTHTXP0_124
MGTHTXN0_124
MGTHTXP1_124
MGTHTXN1_124
MGTHTXP2_124
MGTHTXN2_124
MGTHTXP3_124
MGTHTXN3_124
SZG_PORTB_TX0_P
SZG_PORTB_TX0_N
SZG_PORTB_TX1_P
SZG_PORTB_TX1_N
SZG_PORTA_TX2_P
SZG_PORTA_TX2_N
SZG_PORTA_TX3_P
SZG_PORTA_TX3_N
XCAU7P-1SBVC484I
Title: GPIO Connector
Revision: A0.0
Size: A3
Project: mimas_au_plus.PrjPcb
Date: 17-07-2025
Time: 16:31:34
Sheet 6 of 11
File: GPIO.SchDoc
Numato Lab

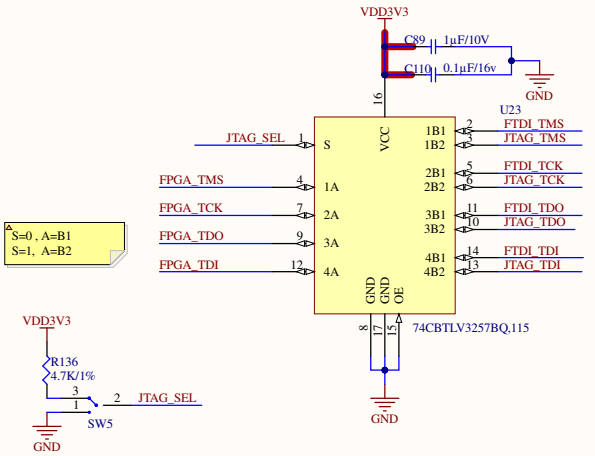
USB-C



FT2232H



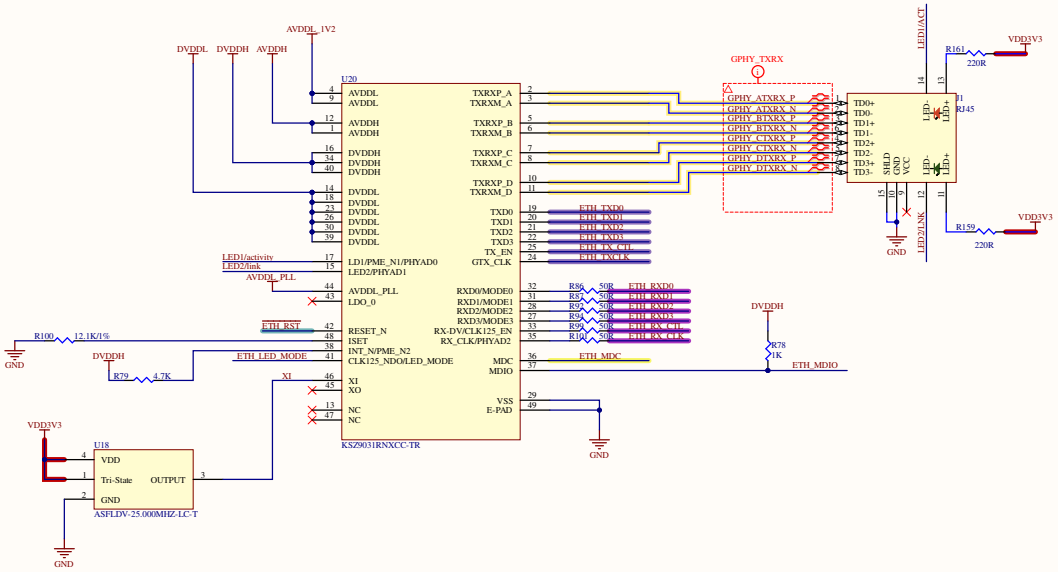




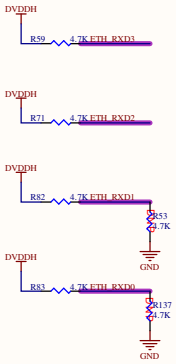
Title:	FT2232H	Revision:	A0.0
Size:	A3	Project:	mimas_au_plus.PrjPcb
Date:	17-07-2025	Time:	16:31:34
Sheet	7 of 11		
File:	FT2232H.SchDoc		

Numato Lab

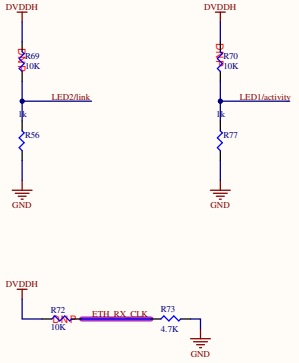
KSZ9031RNX



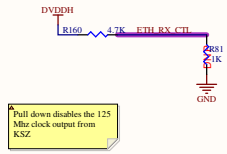
RGMII MODE



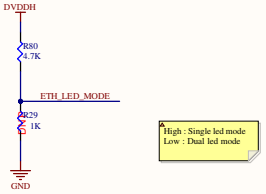
PHY ADD

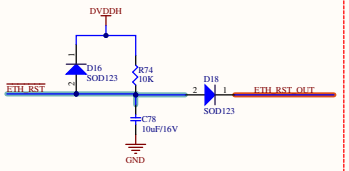


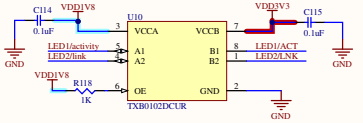
125 Mhz CLOCK OUTPUT ENABLE



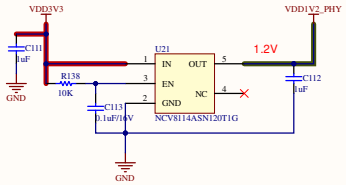
LED mode

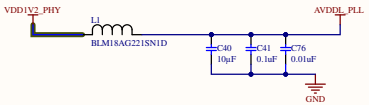


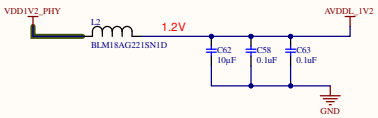


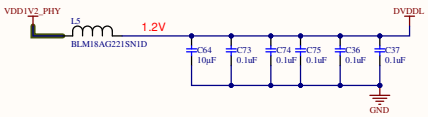


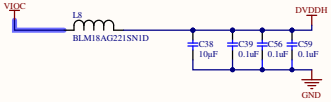
ETH POWER

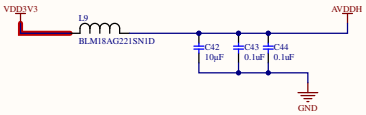






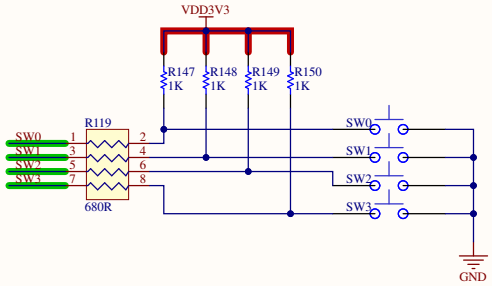




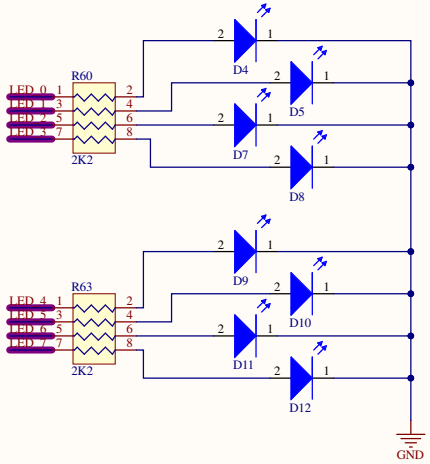


Title: Ethernet PHY		Revision: A0.0	Numato Lab
Size: A2	Project: mimas_au_plus.PrjPcb		
Date: 17-07-2025	Time: 16:31:35	Sheet 8 of 11	
File: Ethernet_PHY.SchDoc			

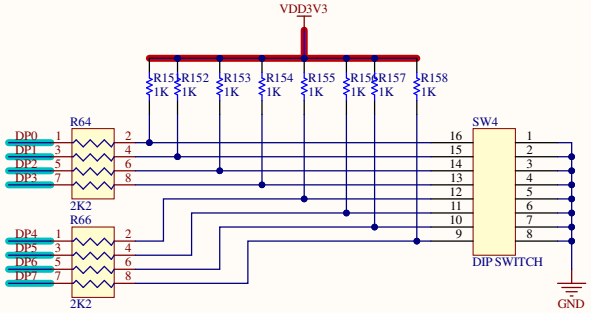
Push Button



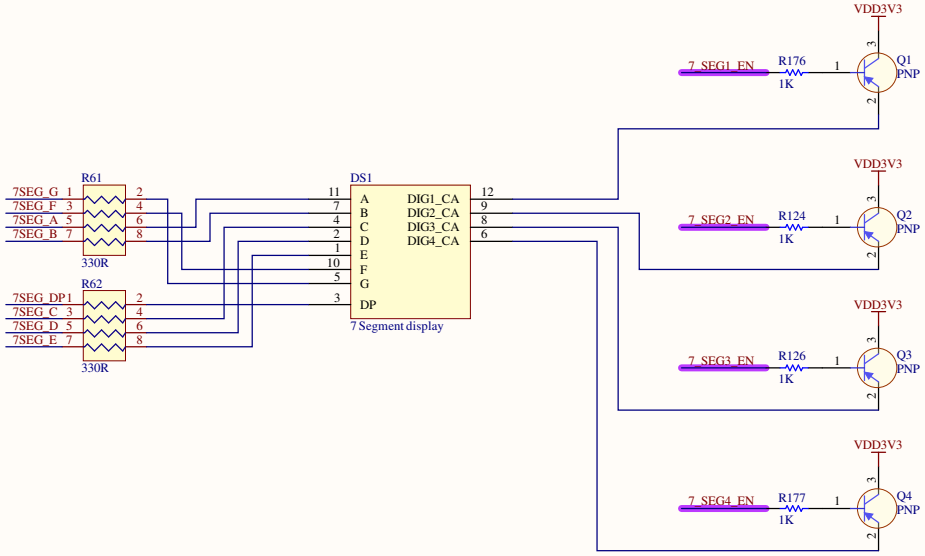
LEDs



DIP Switch



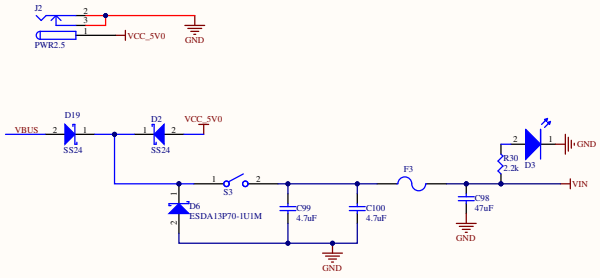
7 Segment Display



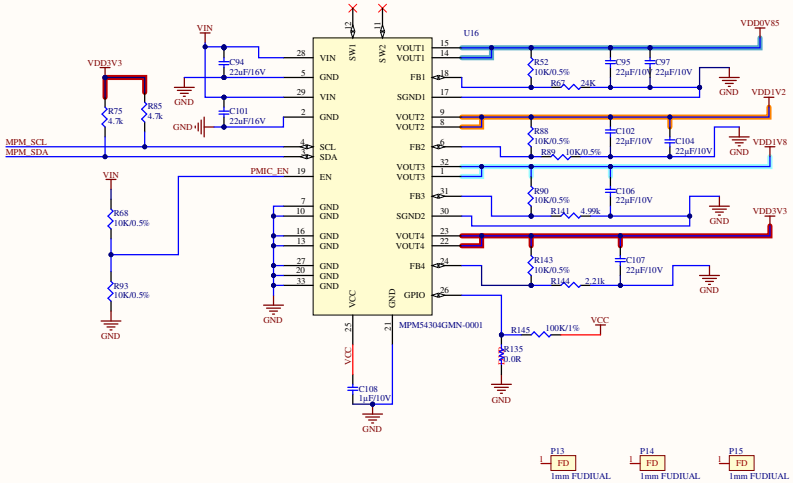
Push Button,DIP Switch,LEDs & 7 Segment Display

Title: 7 Segment Display		Revision: A0.0	Numato Lab
Size: A3	Project: mimas_au_plus.PrjPcb		
Date: 17-07-2025	Time: 16:31:35	Sheet 9 of 11	
File: 7_Segment_Display.SchDoc			

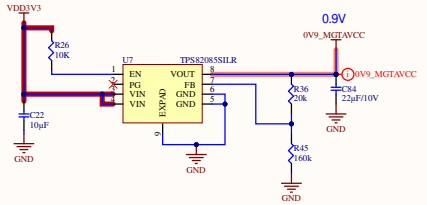
INPUT POWER 5V0



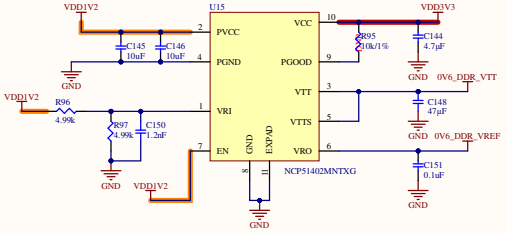
FPGA POWER



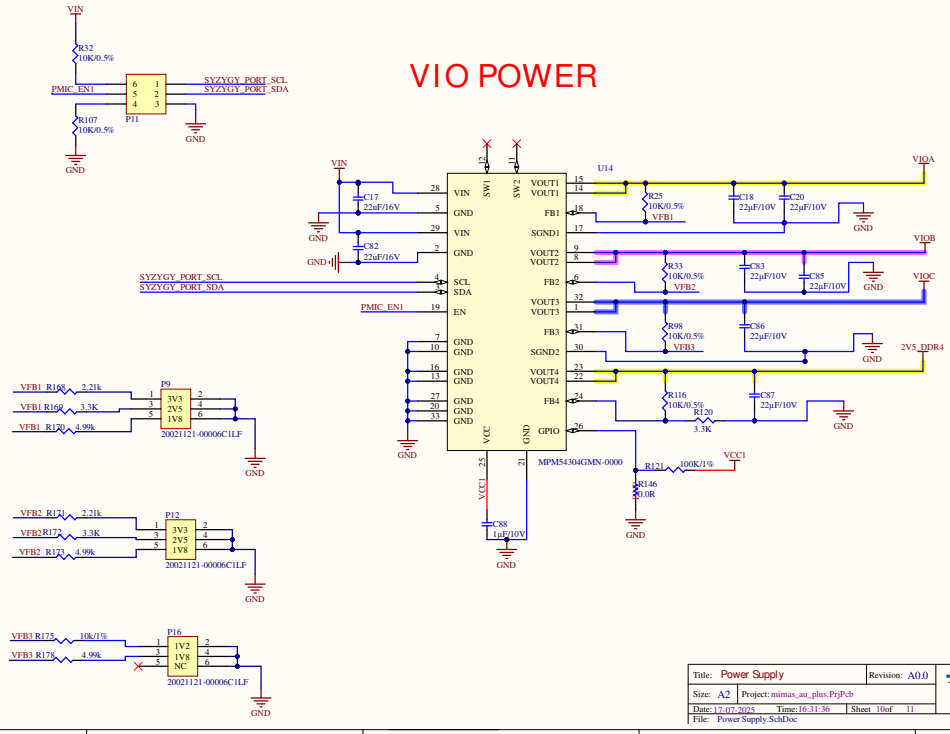
MGTAVCC (0.9V)



DDR4 POWER



VIO POWER



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Size: A2	Project: mimas_au_plus.PrjPcb		
Date: 17-07-2025	Time: 16:31:36	Sheet 10of 11	
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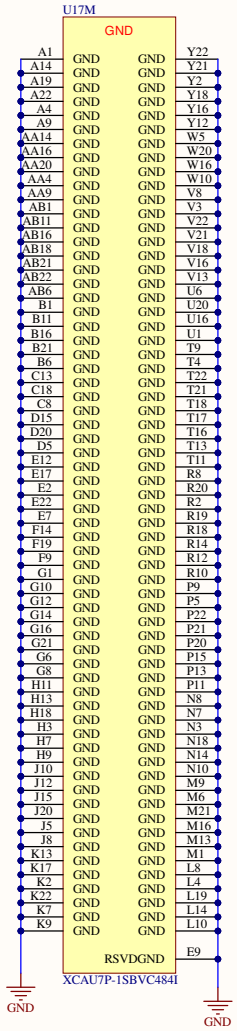
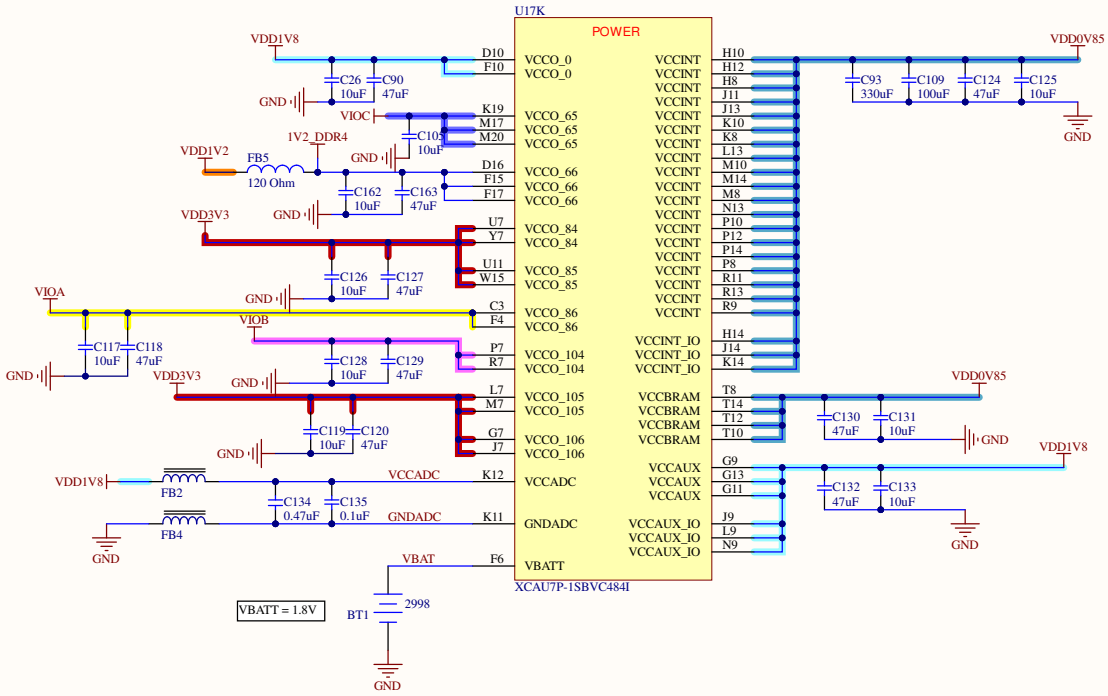
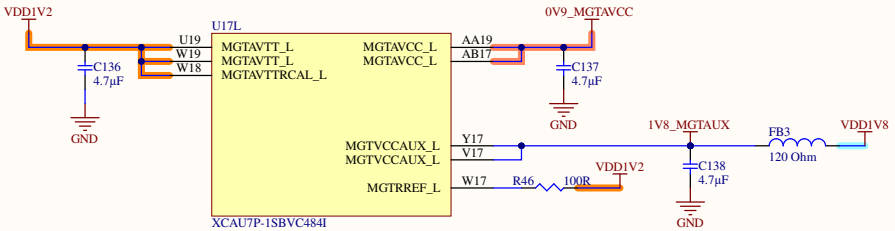
Numato Lab

FPGA POWER







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