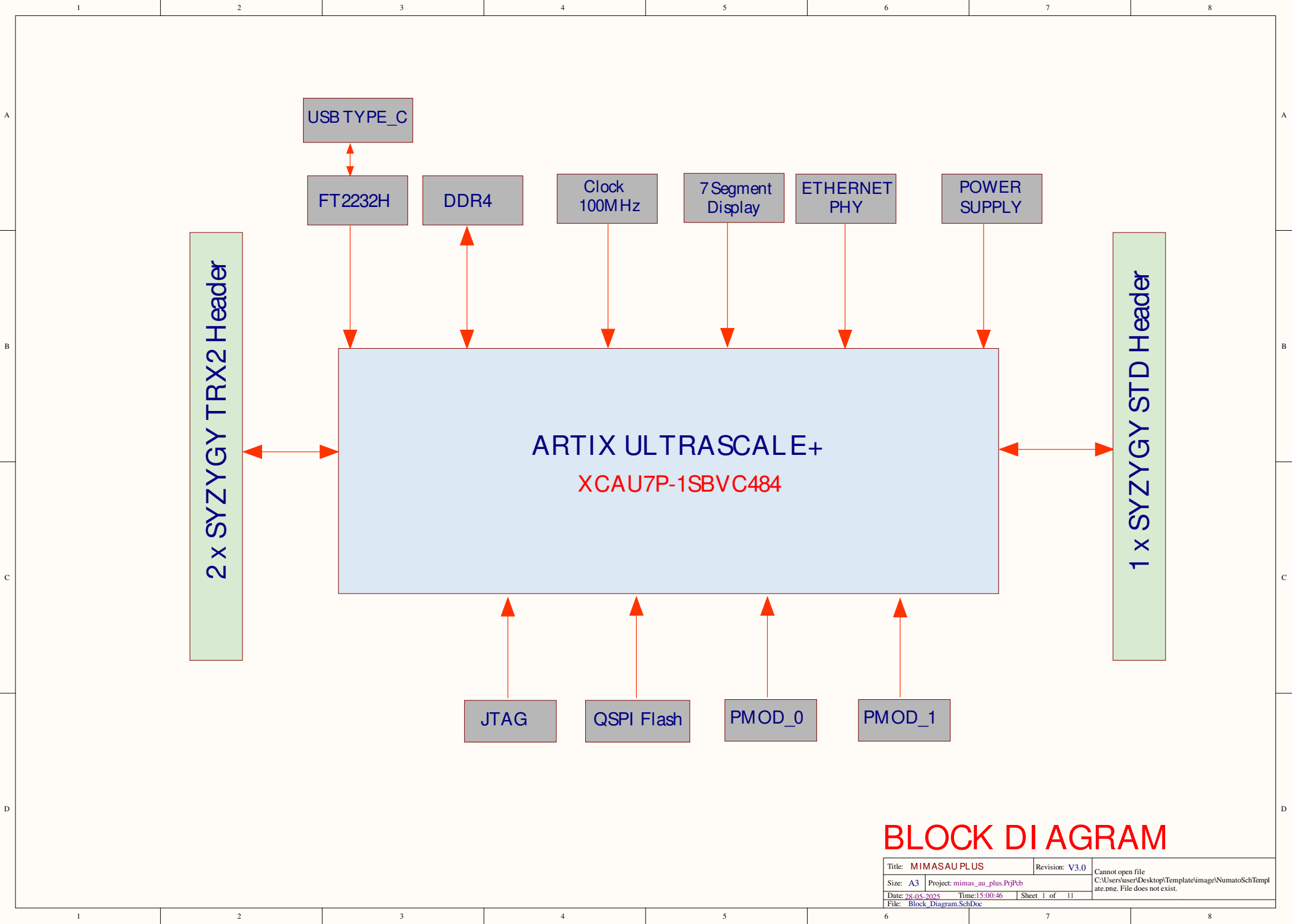
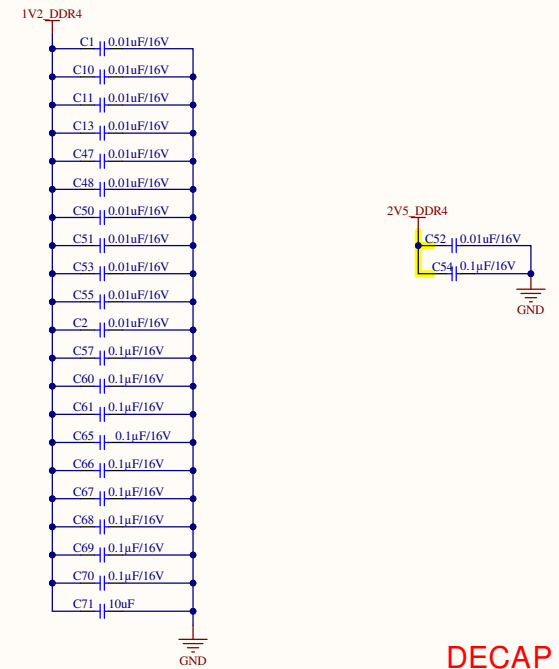
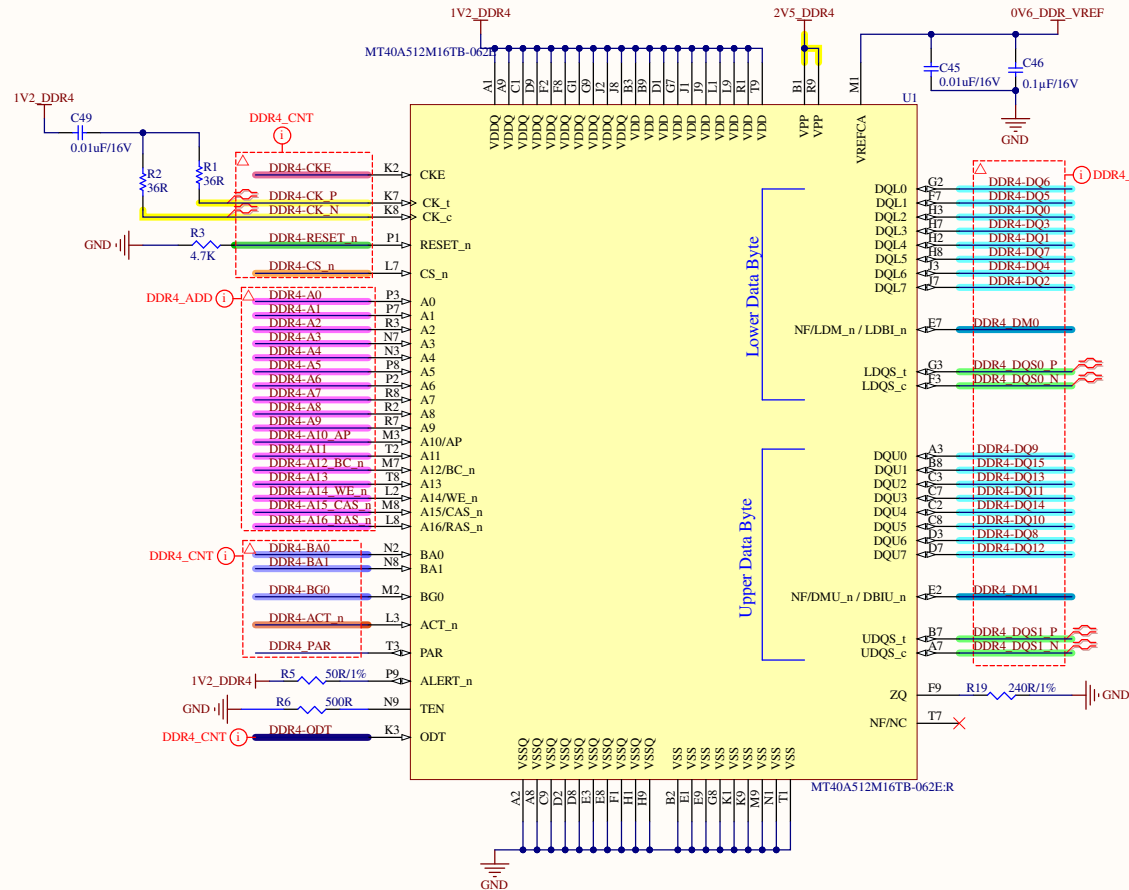




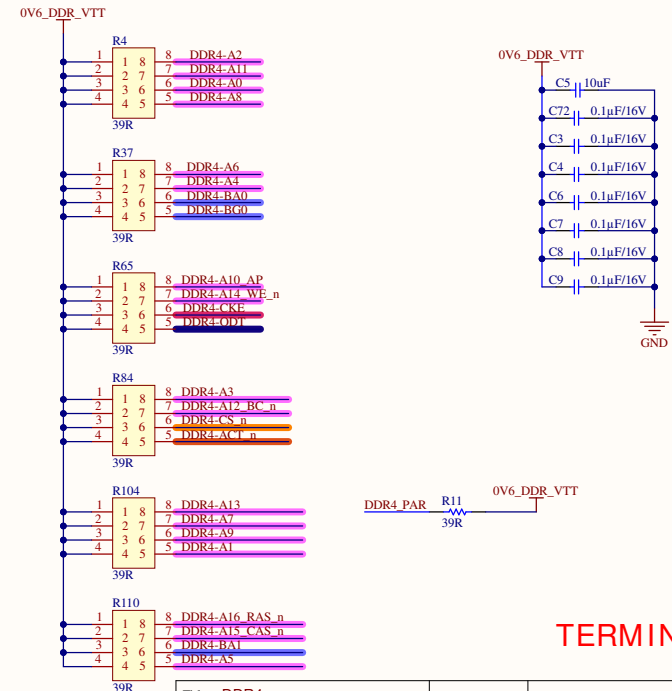
BLOCK DIAGRAM

Title: MIMASAU PLUS		Revision: V3.0		Cannot open file C:\Users\user\Desktop\Template\image\NumatoSchTempl ate.png. File does not exist.
Size: A3	Project: mimas_au_plus.PyJcb			
Date: 28.05.2025	Time: 15:00:46	Sheet 1 of 11		
File: Block_Diagram.SchDoc				

DDR4



DECAP

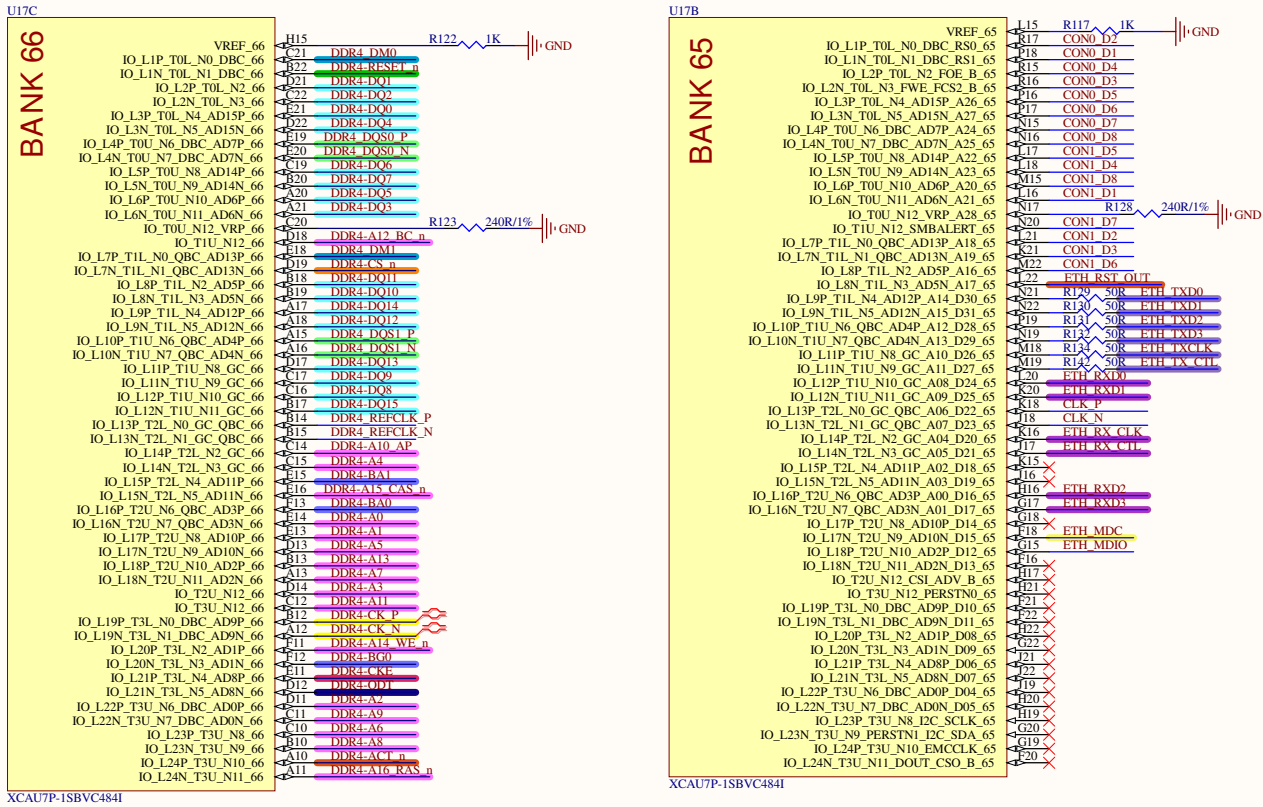


TERMINATION

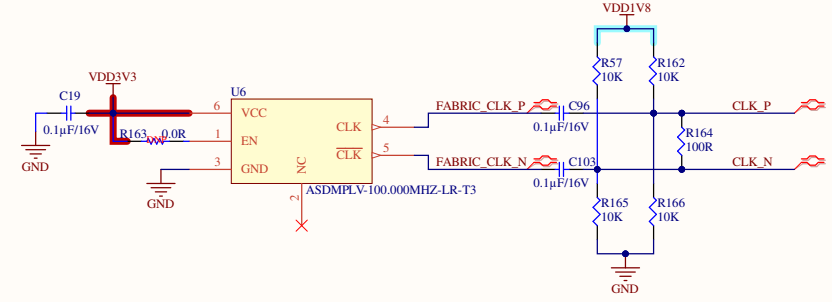
DDR REFERENCE CLOCK 100MHz

Title: DDR4		Revision: V3.0	Cannot open file C:\Users\User\Desktop\Template\image\NumatoSchTempl ate.png. File does not exist.
Size: A3	Project: mimas_au_plus_PrjPcb		
Date: 28.05.2025	Time: 15:00:46	Sheet 2 of 11	
File: DDR4_SchDoc			

HP BANKS

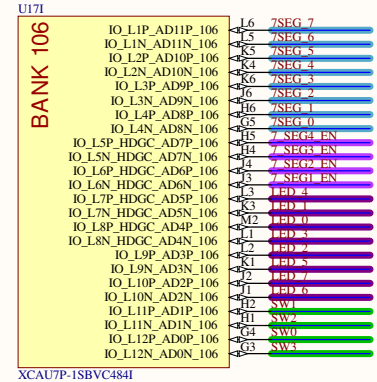
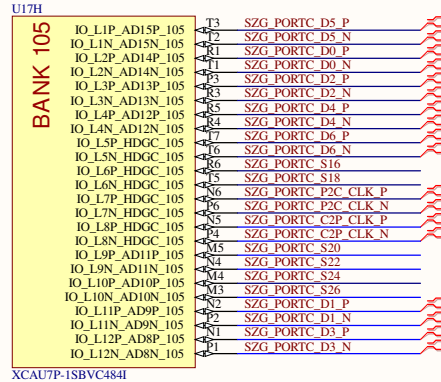
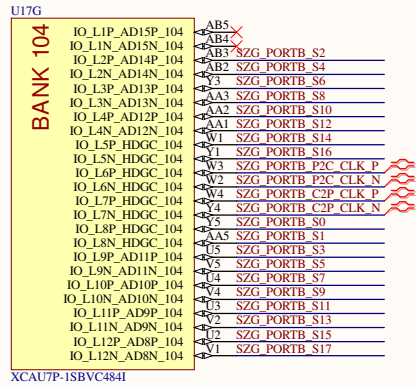
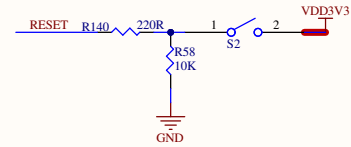
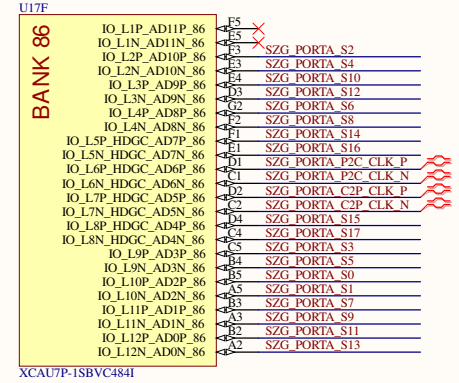
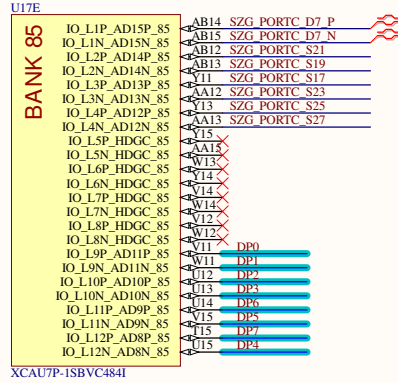
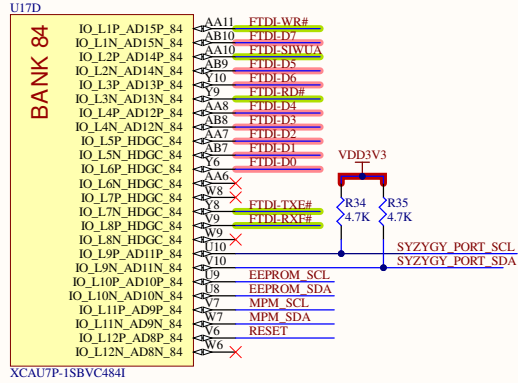


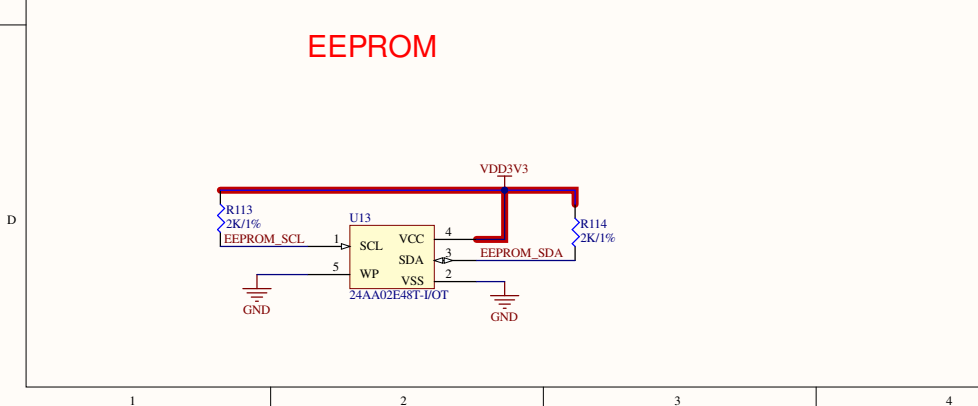
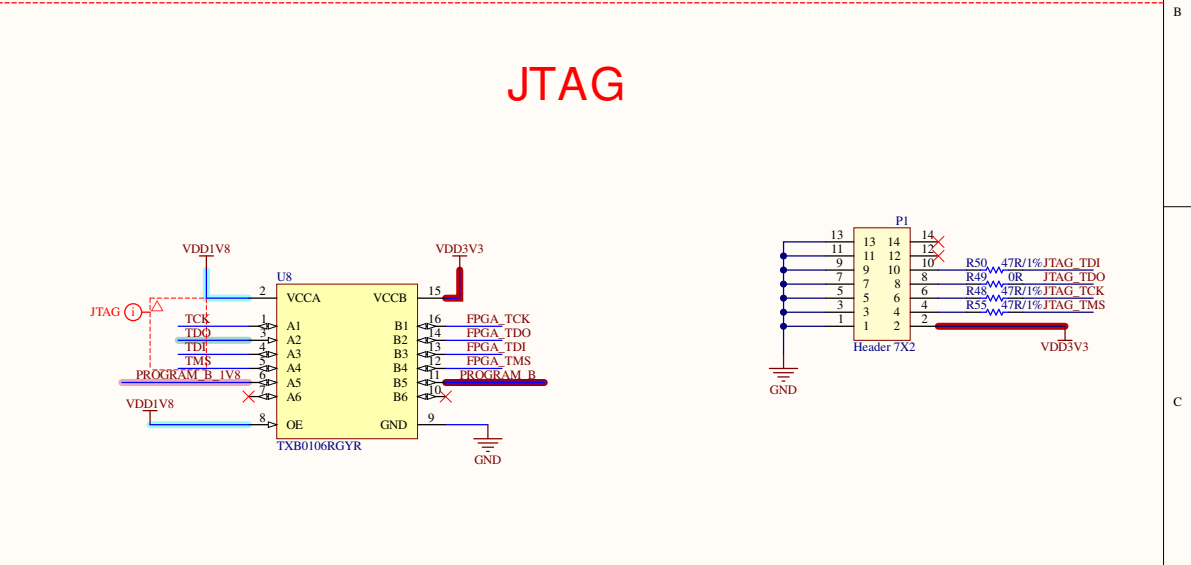
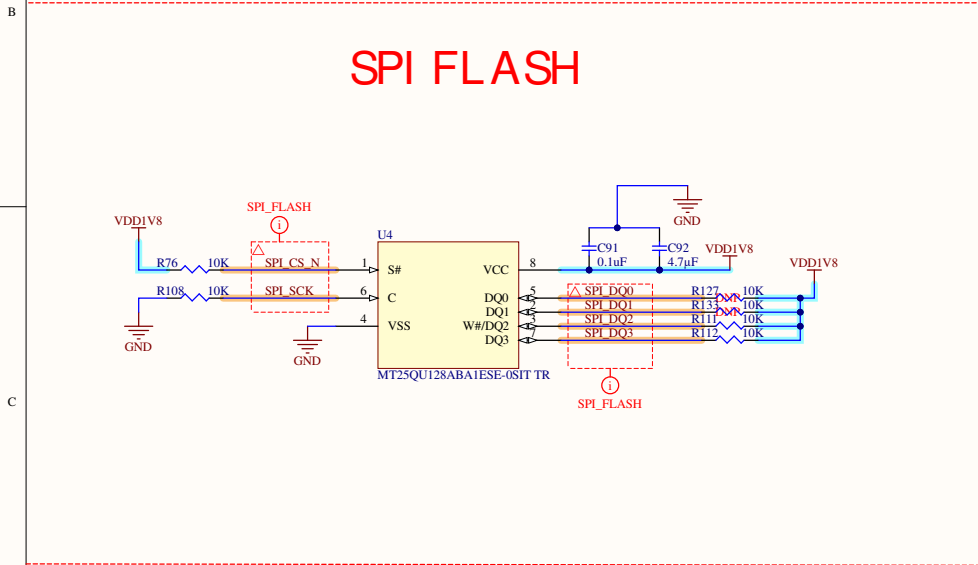
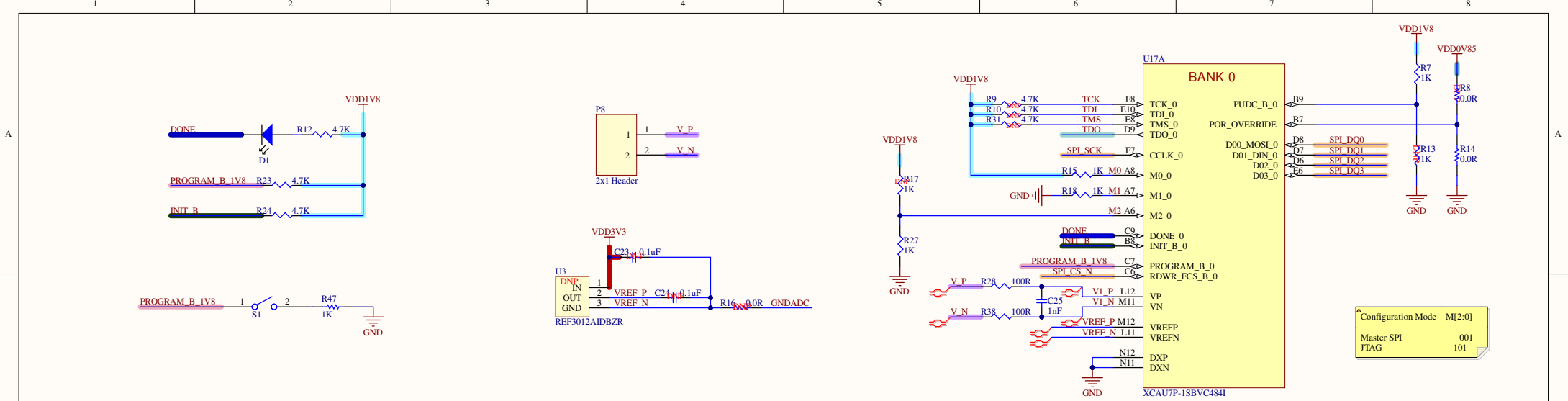
FABRIC CLOCK 100MHz



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Size: A3	Project: mimas_au_plus.PyJcb	C:\Users\user\Desktop\Template\image\NumatoSchTempl
Date: 28.05.2025	Time: 15:00:46	Sheet 3 of 11
File: FPGA_A.SchDoc		ate.png. File does not exist.

HD BANKS



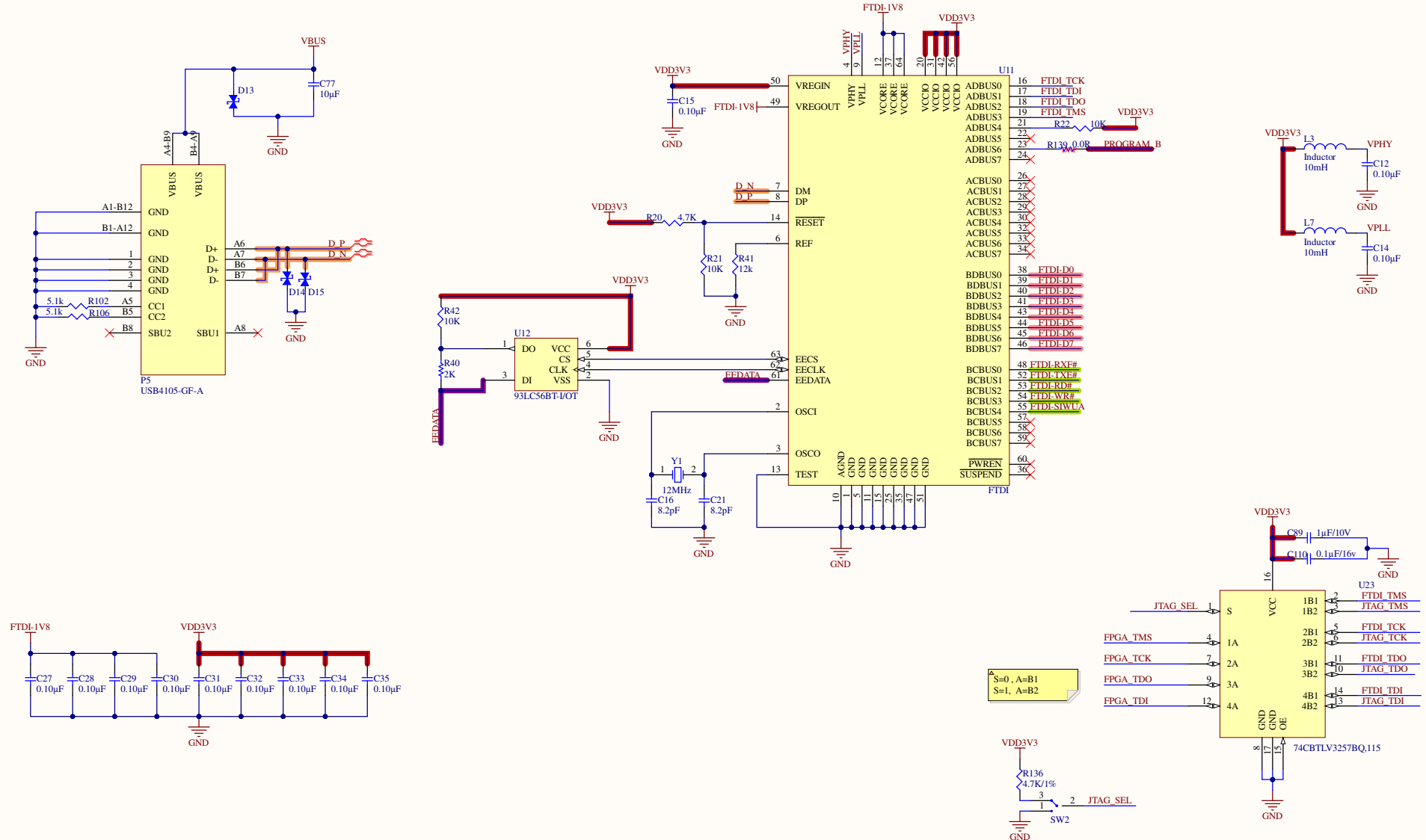


FPGA Configuration

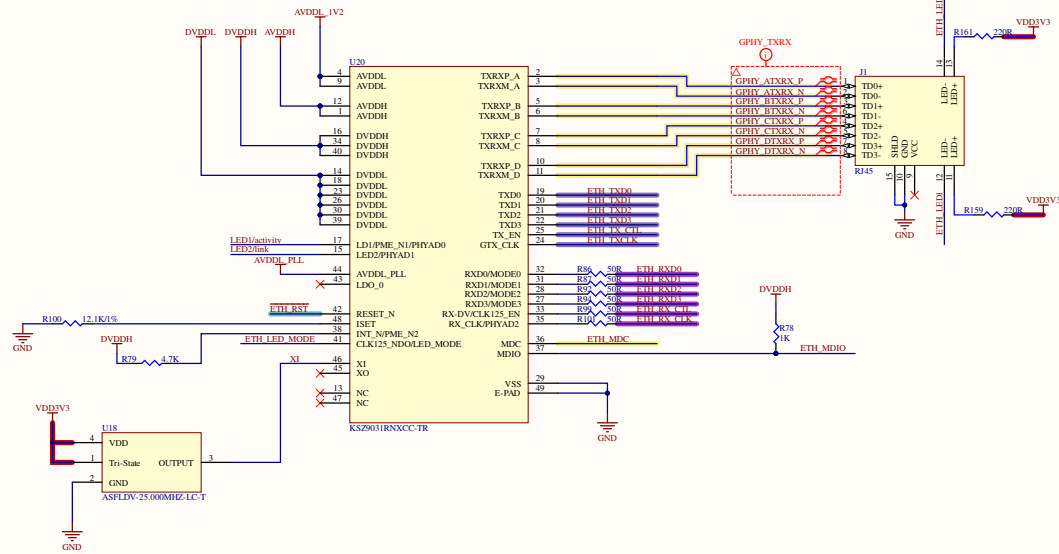
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Size: A3	Project: mimas_au_plus.PjPcb	C:\Users\user\Desktop\Template\image\NumatoSchTempl
Date: 28.05.2025	Time: 15:00:47	ate.png. File does not exist.
File: FPGA_C.SchDoc	Sheet 5 of 11	

USB-C

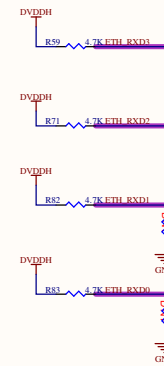
FT2232H



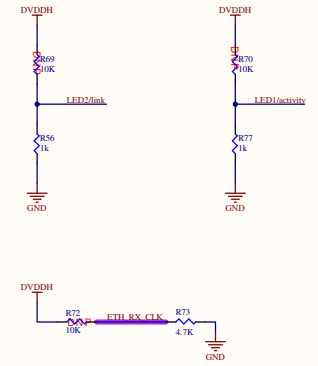
KSZ9031 RN X



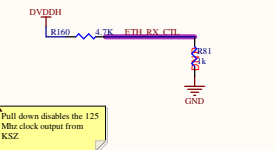
RGM II MODE



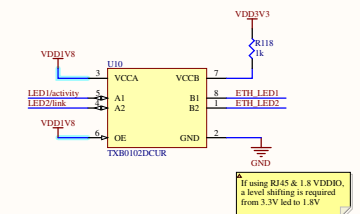
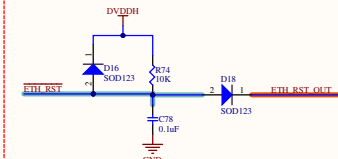
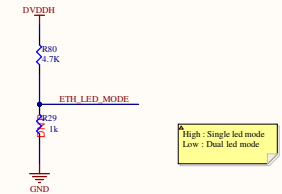
PHY ADD



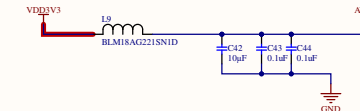
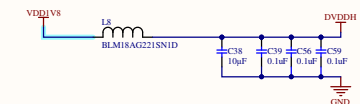
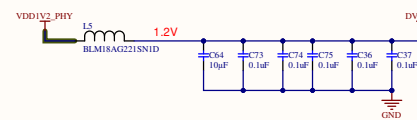
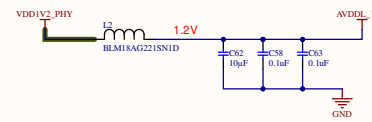
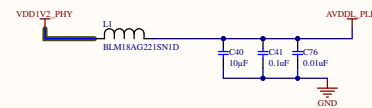
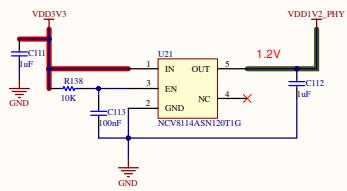
125 Mhz CLOCK OUTPUT ENABLE



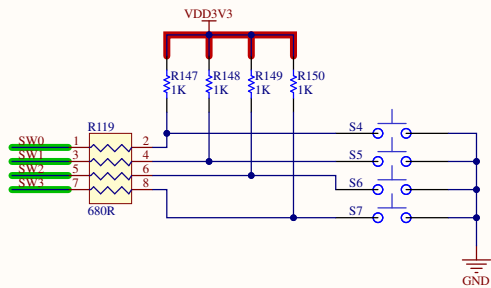
LED mode



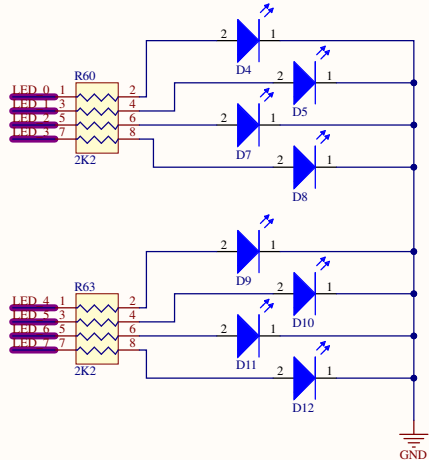
ETH POWER



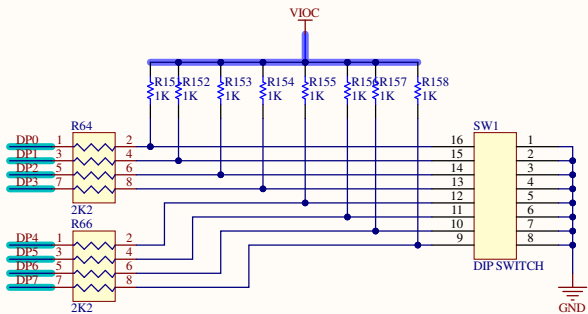
Push Button



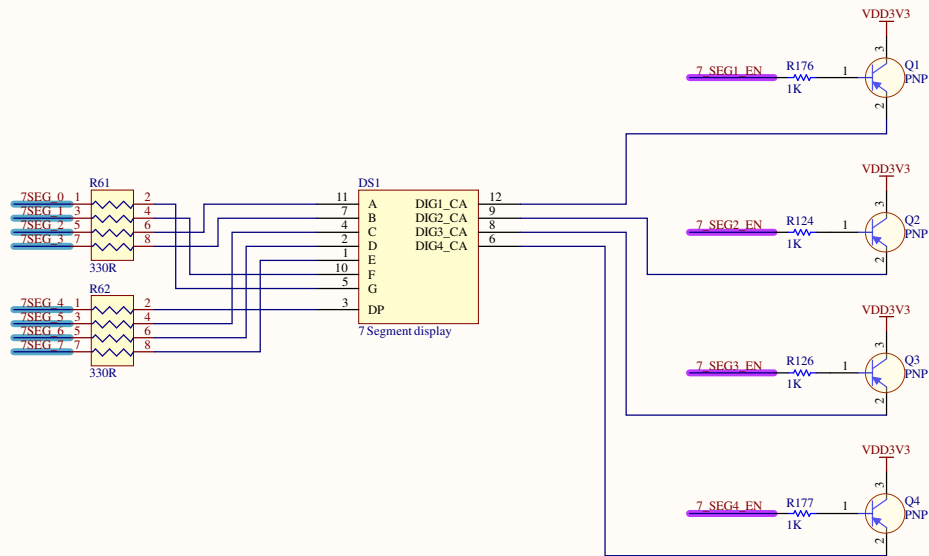
LEDs



DIP Switch



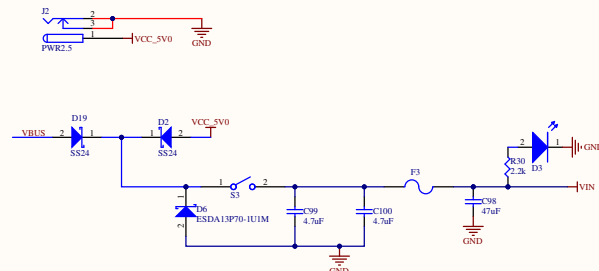
7 Segment Display



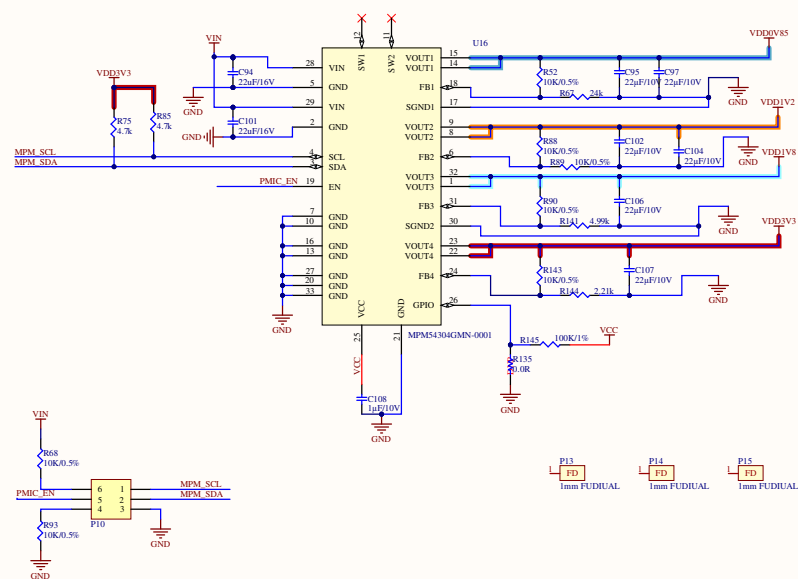
Push Button,DIP Switch,LEDs & 7 Segment Display

Title: 7 Segment Display	Revision: V3.0	Cannot open file
Size: A3	Project: mimas_au_plus.PyJcb	C:\Users\user\Desktop\Template\image\NumatoSchTemplate.png. File does not exist.
Date: 28-05-2025	Time: 15:00:47	Sheet 9 of 11
File: 7_Segment_Display.SchDoc		

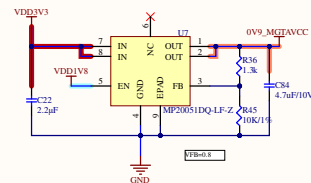
INPUT POWER 5V0



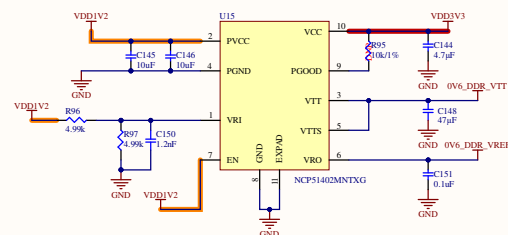
FPGA POWER



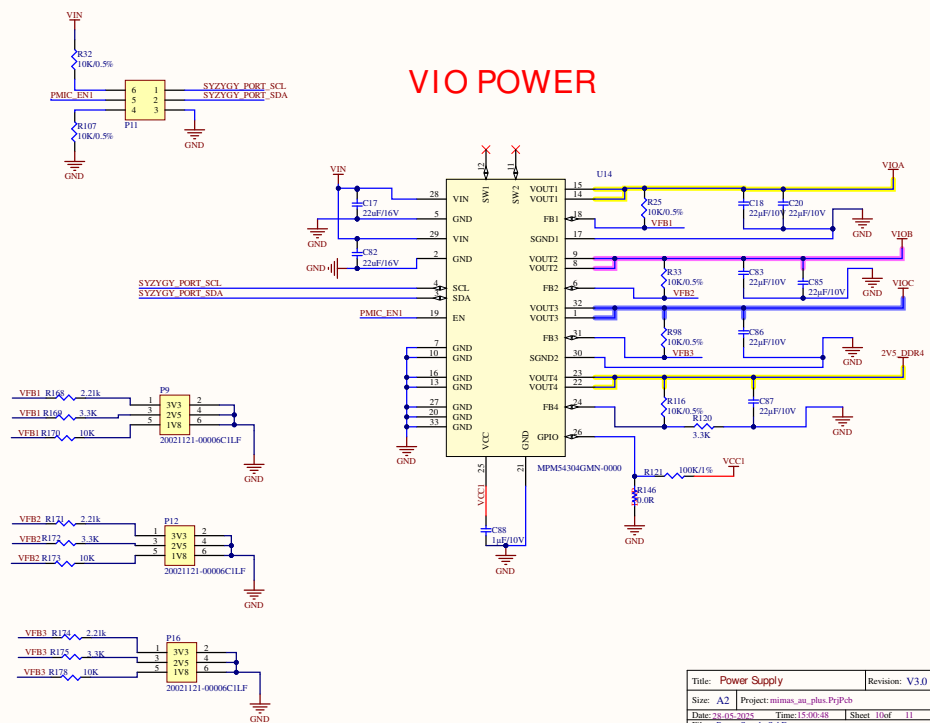
MGTAVCC (0.9V)



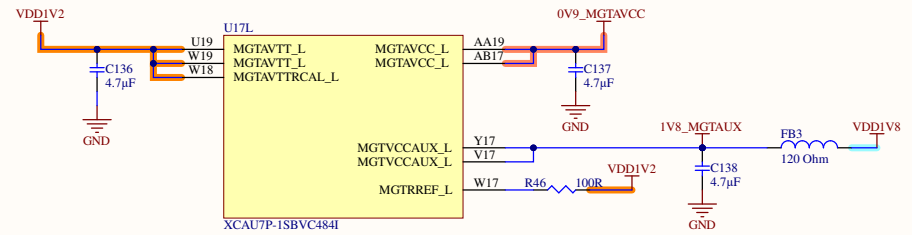
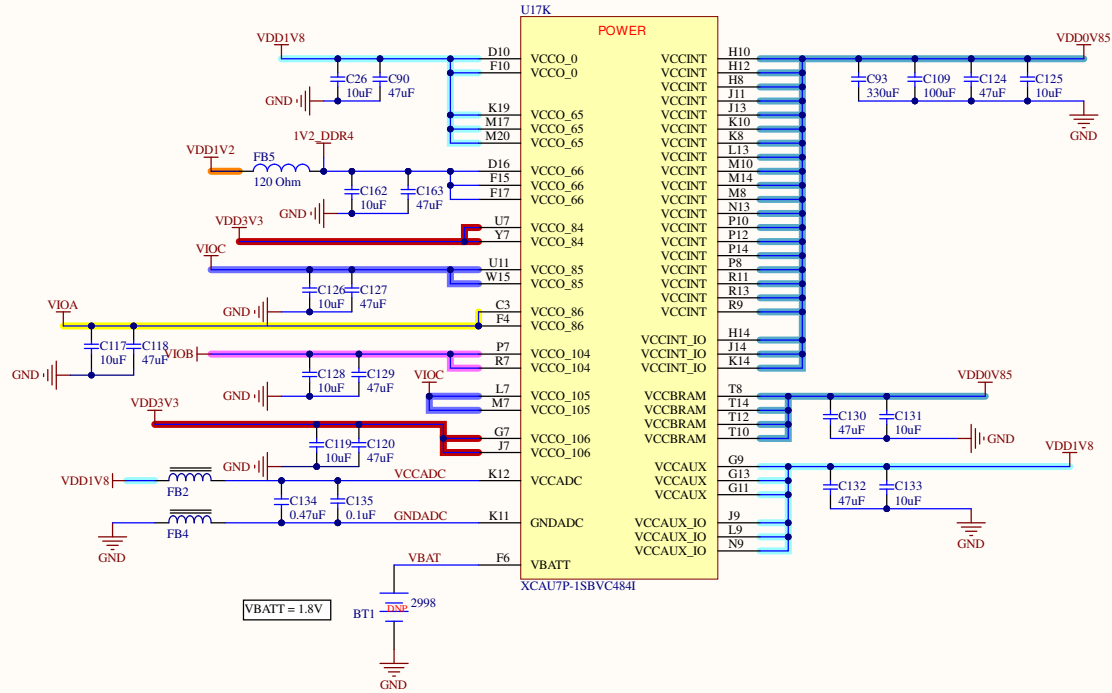
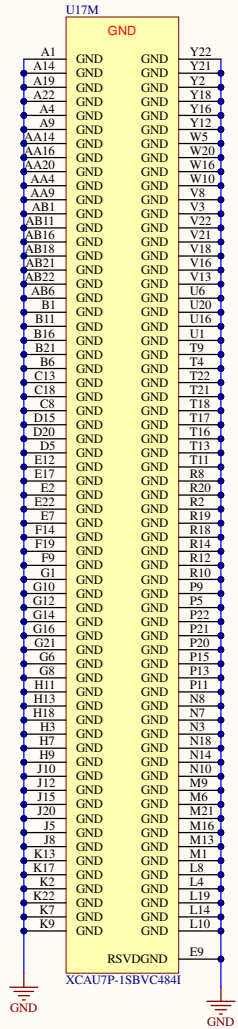
DDR4 POWER



VIO POWER



FPGA POWER



Title: FPGA_PWR		Revision: V3.0	Cannot open file C:\Users\user\Desktop\Template\image\NumatoSchTempl ate.png. File does not exist.
Size: A3	Project: mimas_au_plus.PrjPcb		
Date: 28-05-2025	Time: 15:00:48	Sheet 11 of 11	
File: FPGA_PWR.SchDoc			