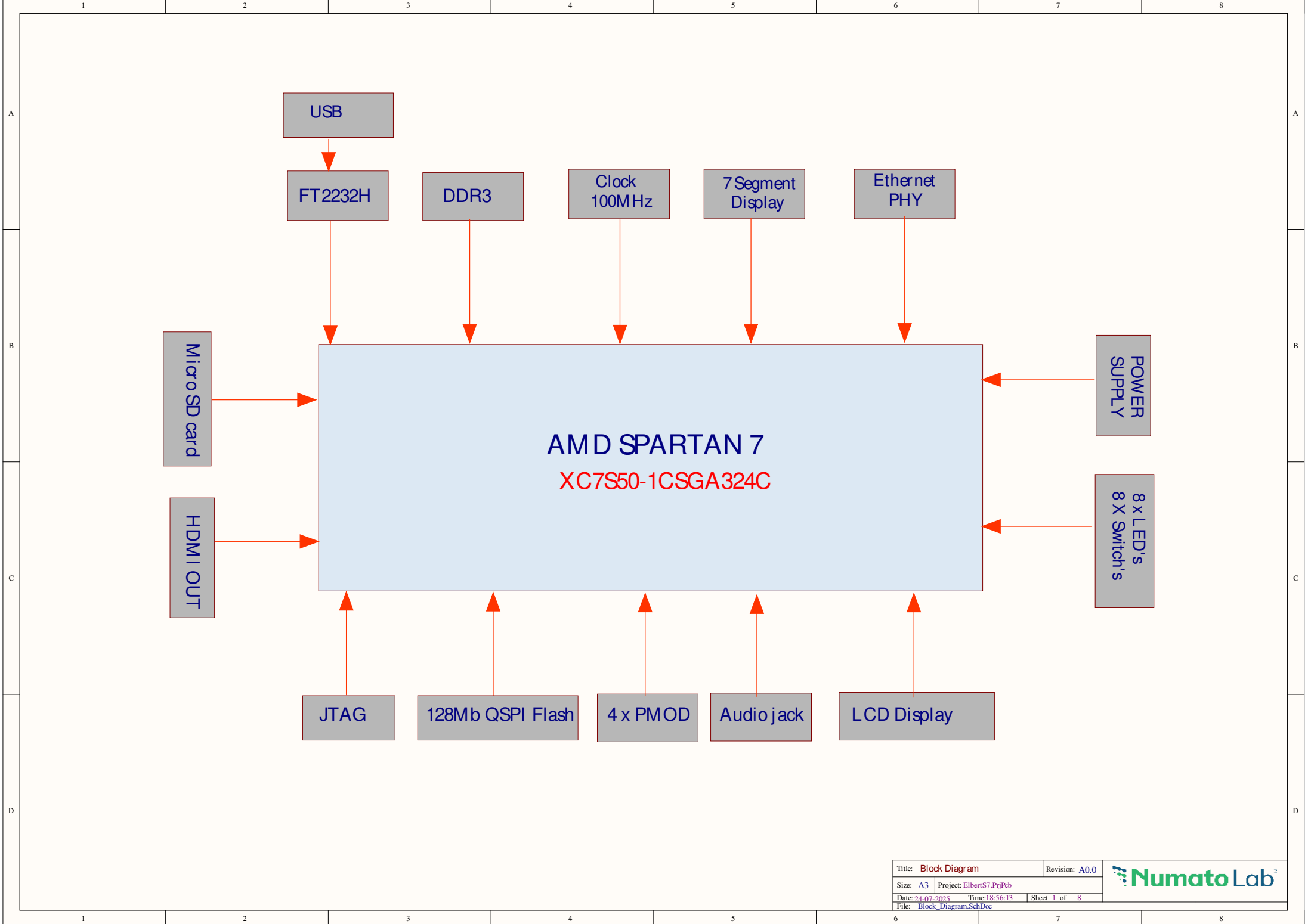
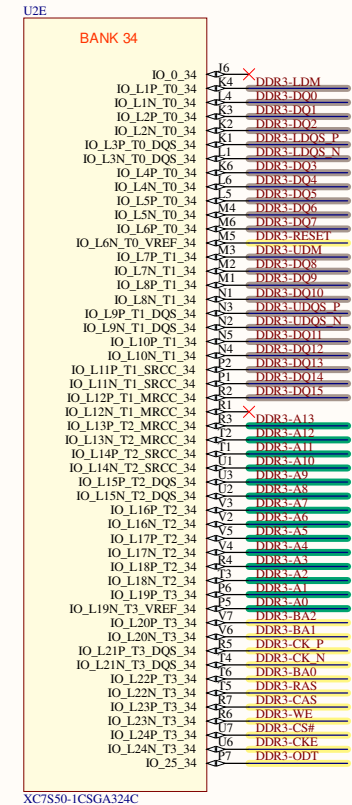
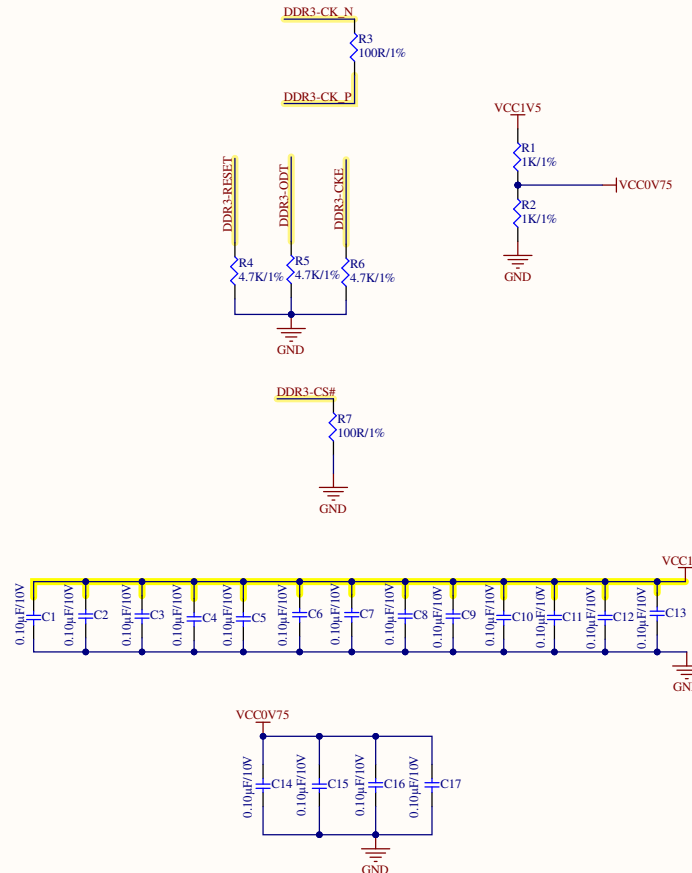
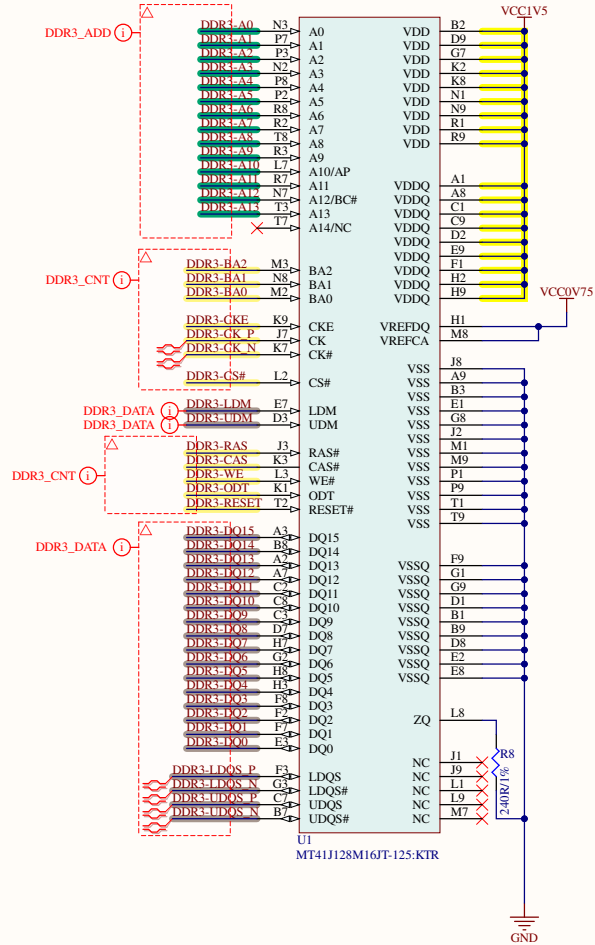
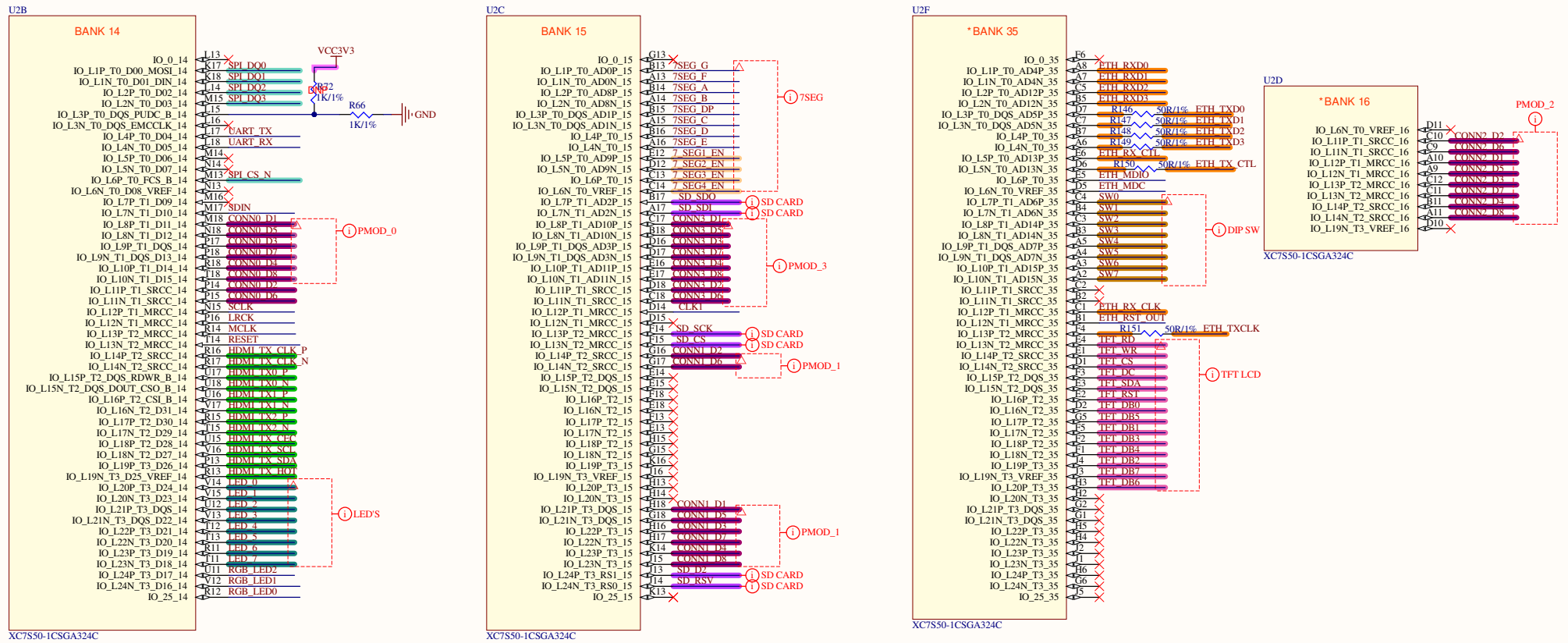




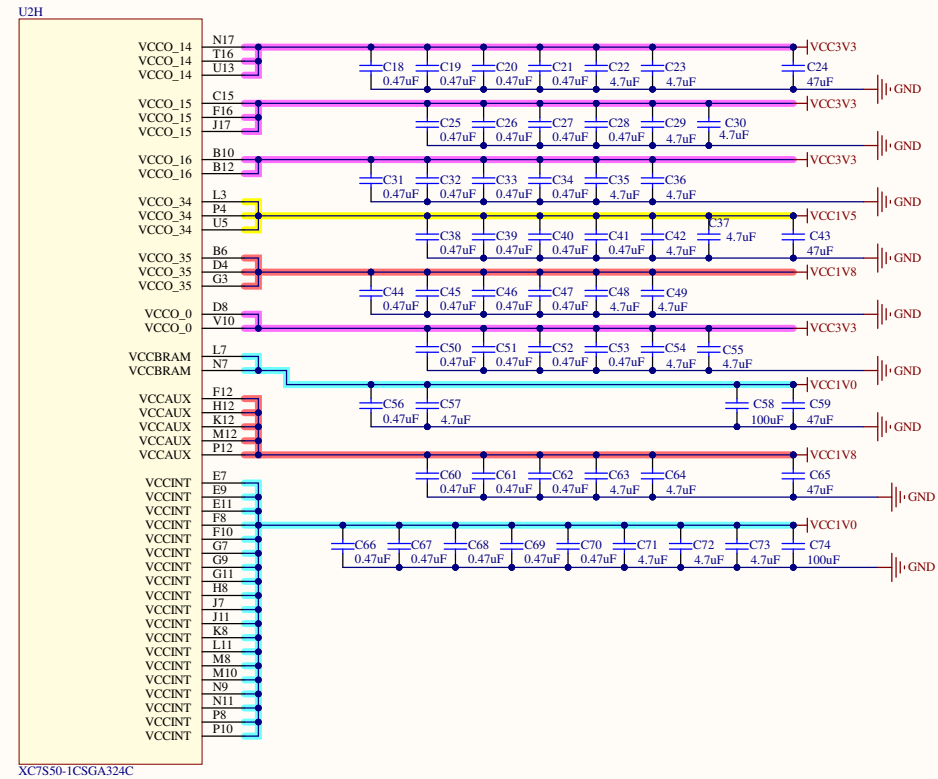
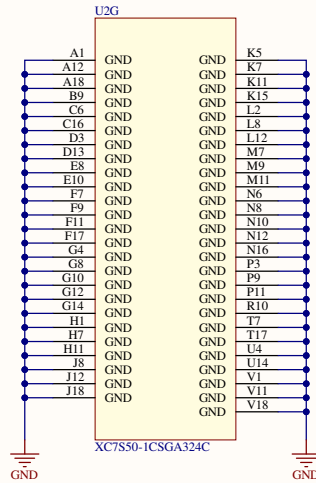
DDR3



FPGA Banks



FPGA Power



A



C



D

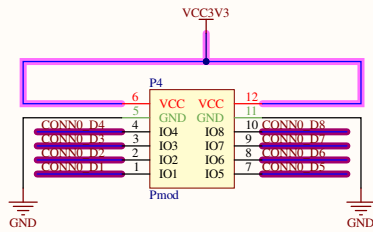


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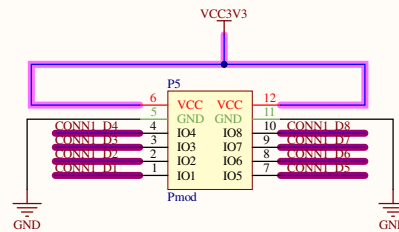


6	7	8
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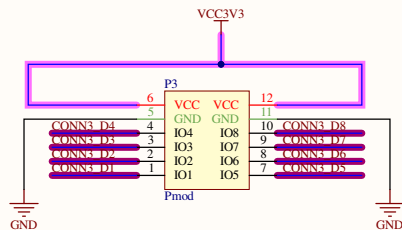
PMOD_0



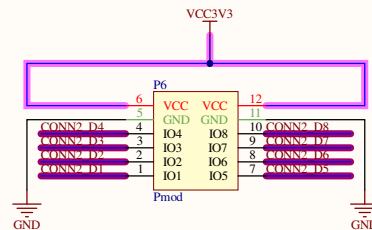
PMOD_1



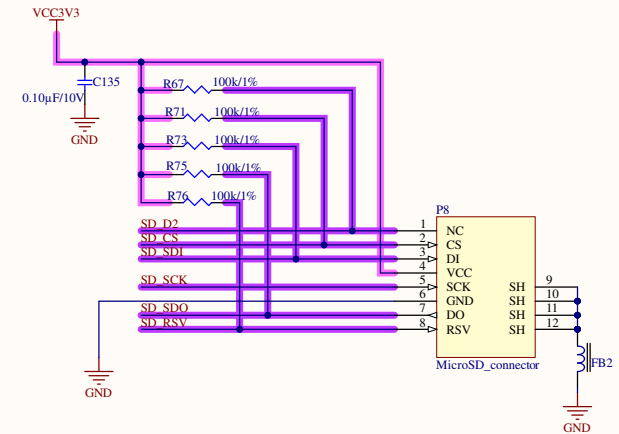
PMOD_3



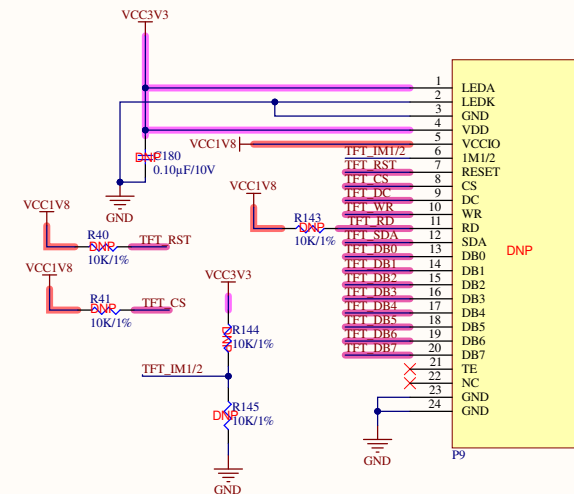
PMOD_2



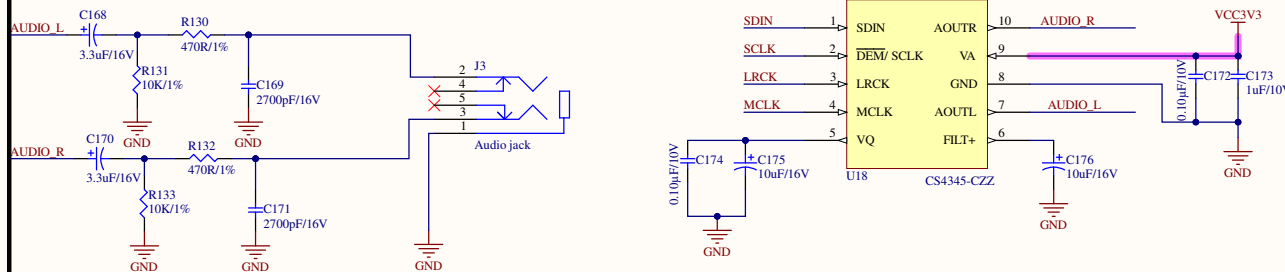
MicroSD



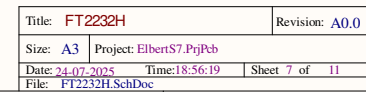
LCD DISPLAY



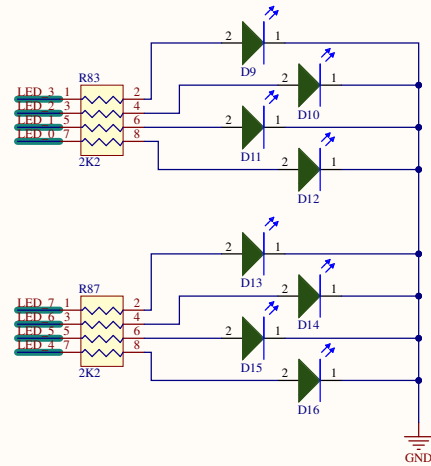
AUDIO JACK



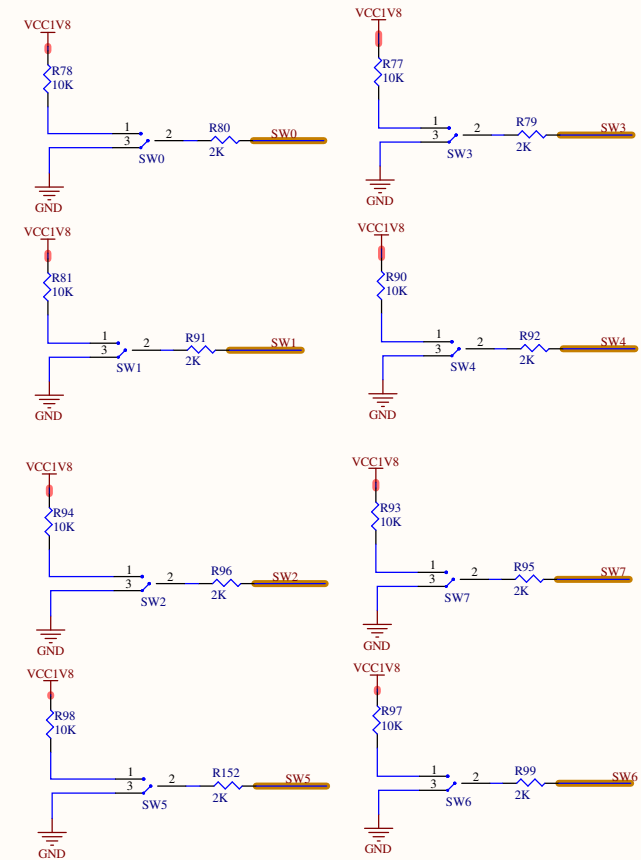
FT 2232H



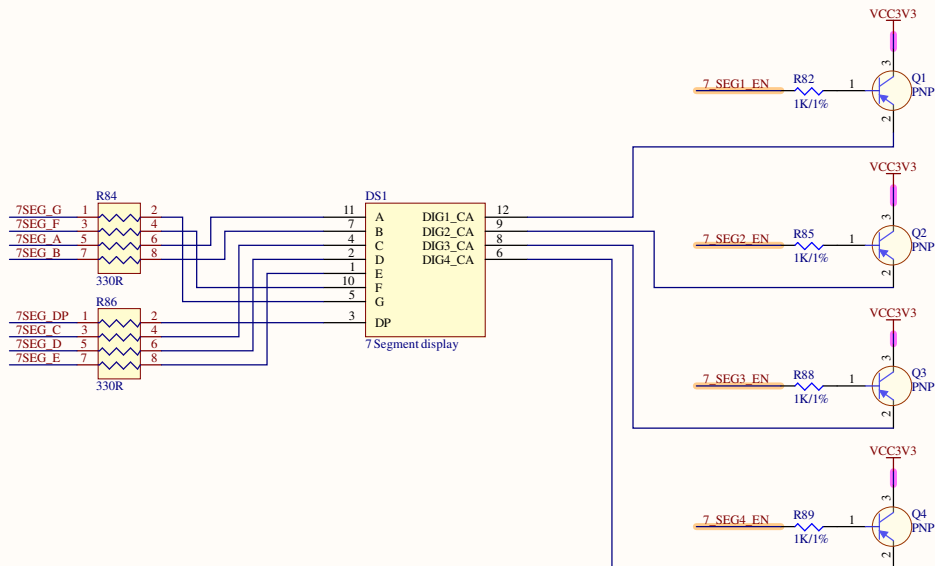
LEDs



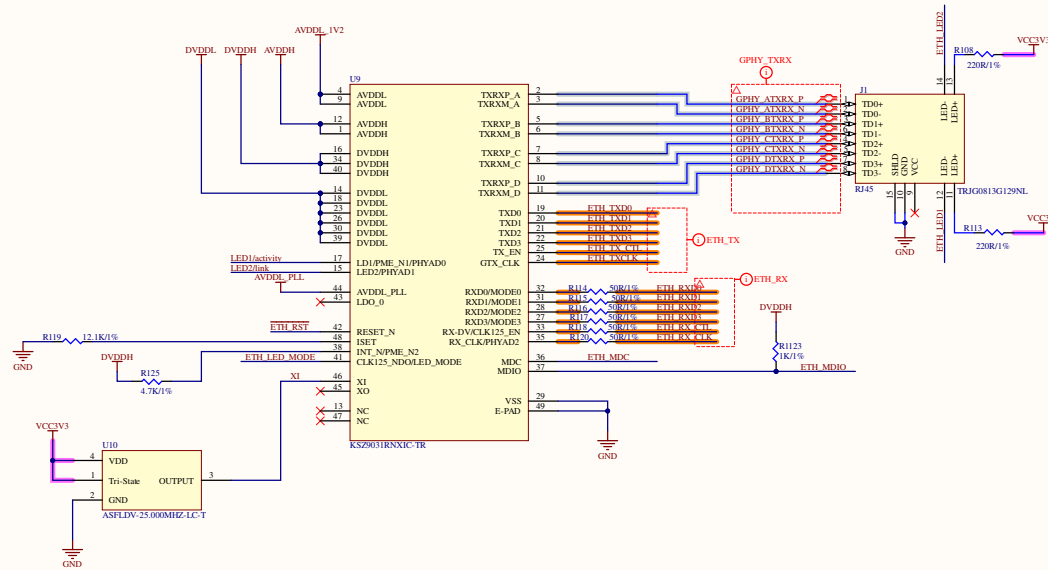
Switch



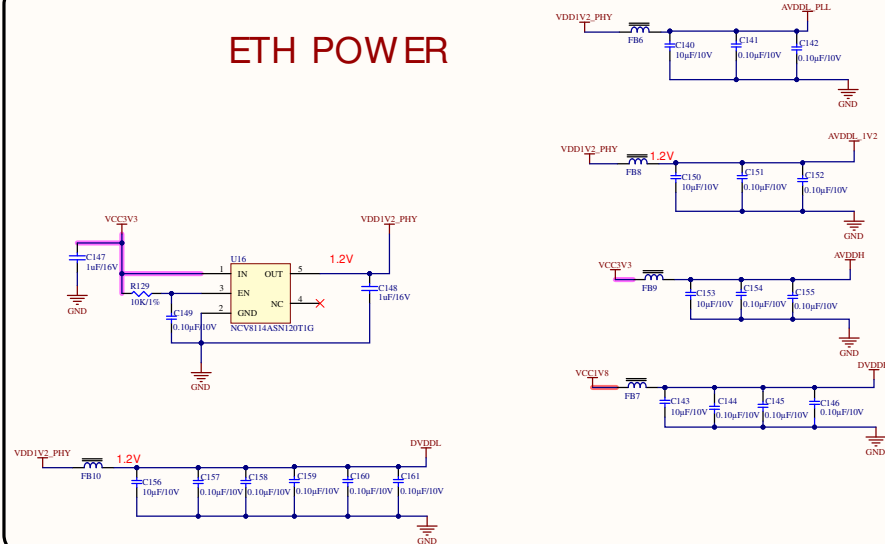
7 Segment Display



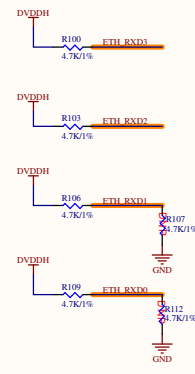
KSZ9031RNX



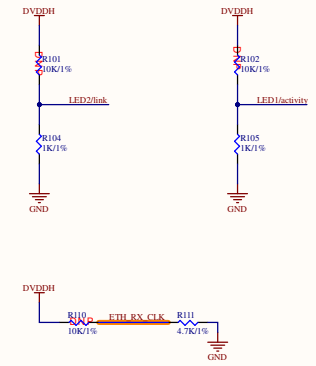
ETH POWER



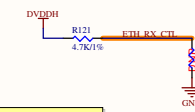
RGM II MODE



PHY ADD

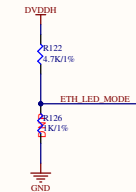


125 Mhz CLOCK OUTPUT ENABLE

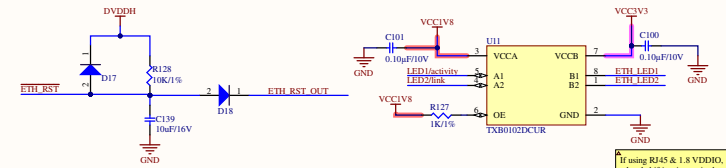


Pull down disables the 125 Mhz clock output from KSZ.

LED mode



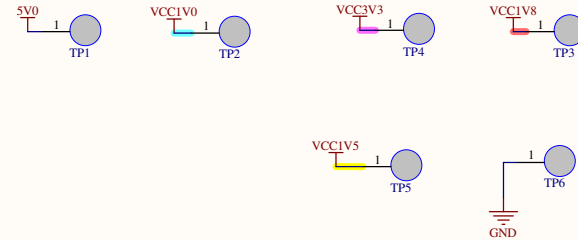
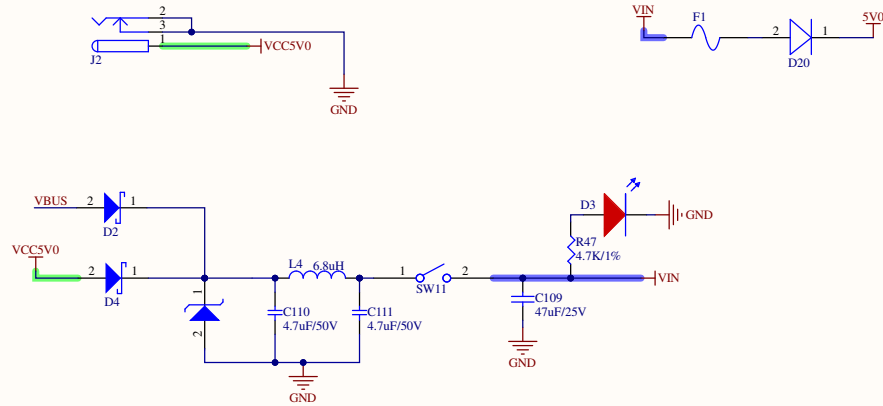
High : Single led mode
Low : Dual led mode



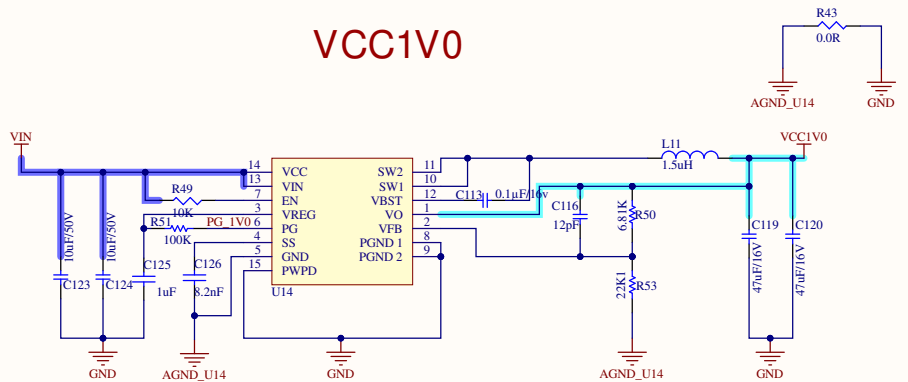
If using RJ45 & 1.8 VDDIO, a level shifting is required from 3.3V led to 1.8V

[illegible]

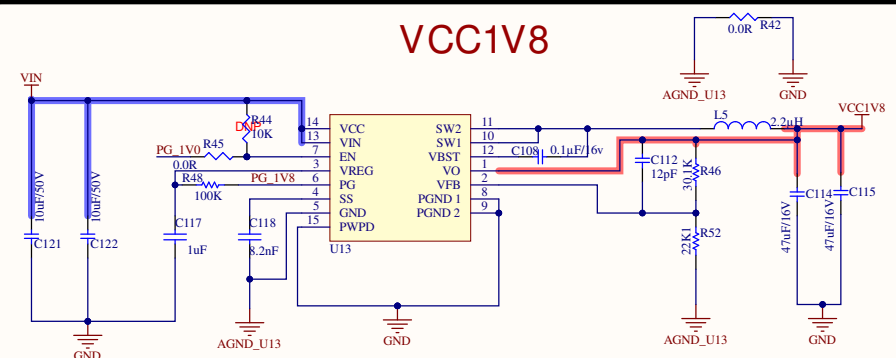
DC Jack



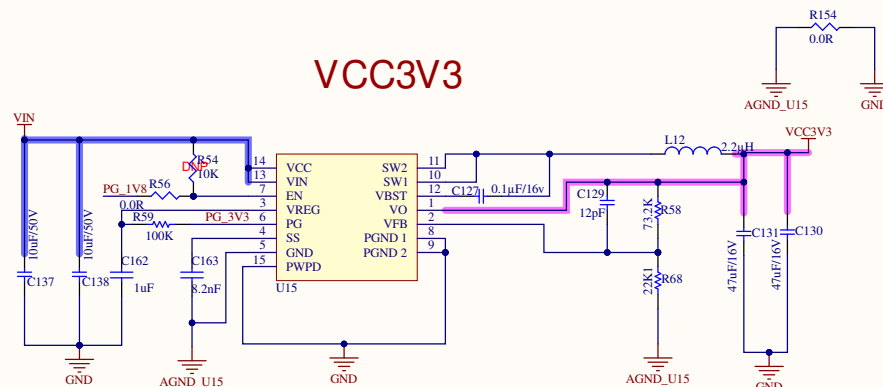
VCC1V0



VCC1V8



VCC3V3



VCC1V5

