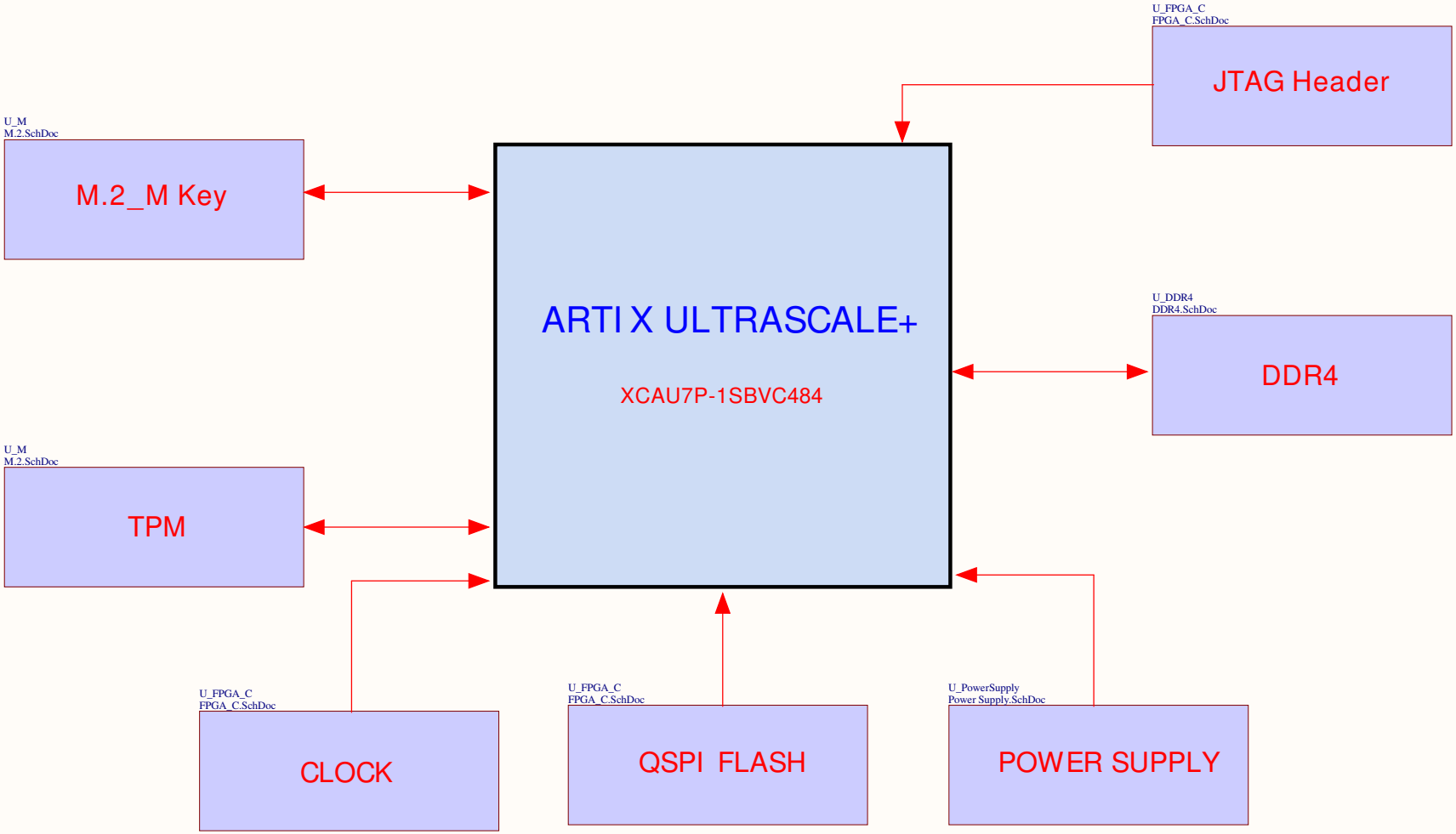

Block Diagram

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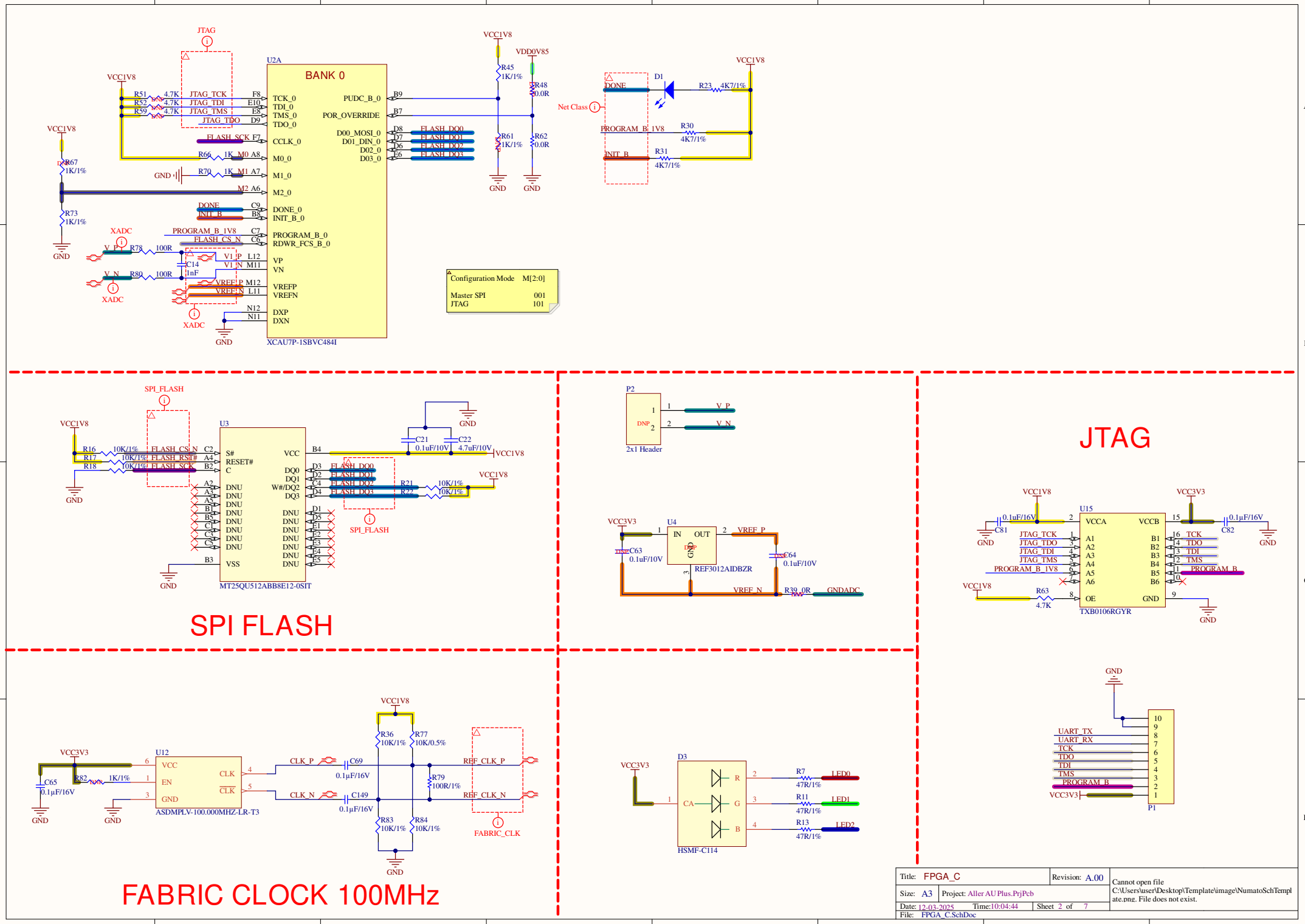
Date: 12-03-2025	Time: 10:04:43	Sheet 1 of 7	
File: BlockDiagram.SchDoc			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U2A
BANK 0
XCAU7P-1SBVC484I
Configuration Mode M[2:0]
Master SPI 001
JTAG 101
SPI_FLASH
U3
MT25QU512ABB8E12-0SIT
SPI FLASH
P2
2x1 Header
U4
REF3012AIDBZR
JTAG
U15
TXB0106RGYR
U12
ASDMPLV-100.000MHZ-LR-T3
FABRIC CLOCK 100MHz
D3
HSMF-C114
P1
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Revision: A.00
Size: A3
Project: Aller AU Plus.PrjPcb
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Sheet 2 of 7
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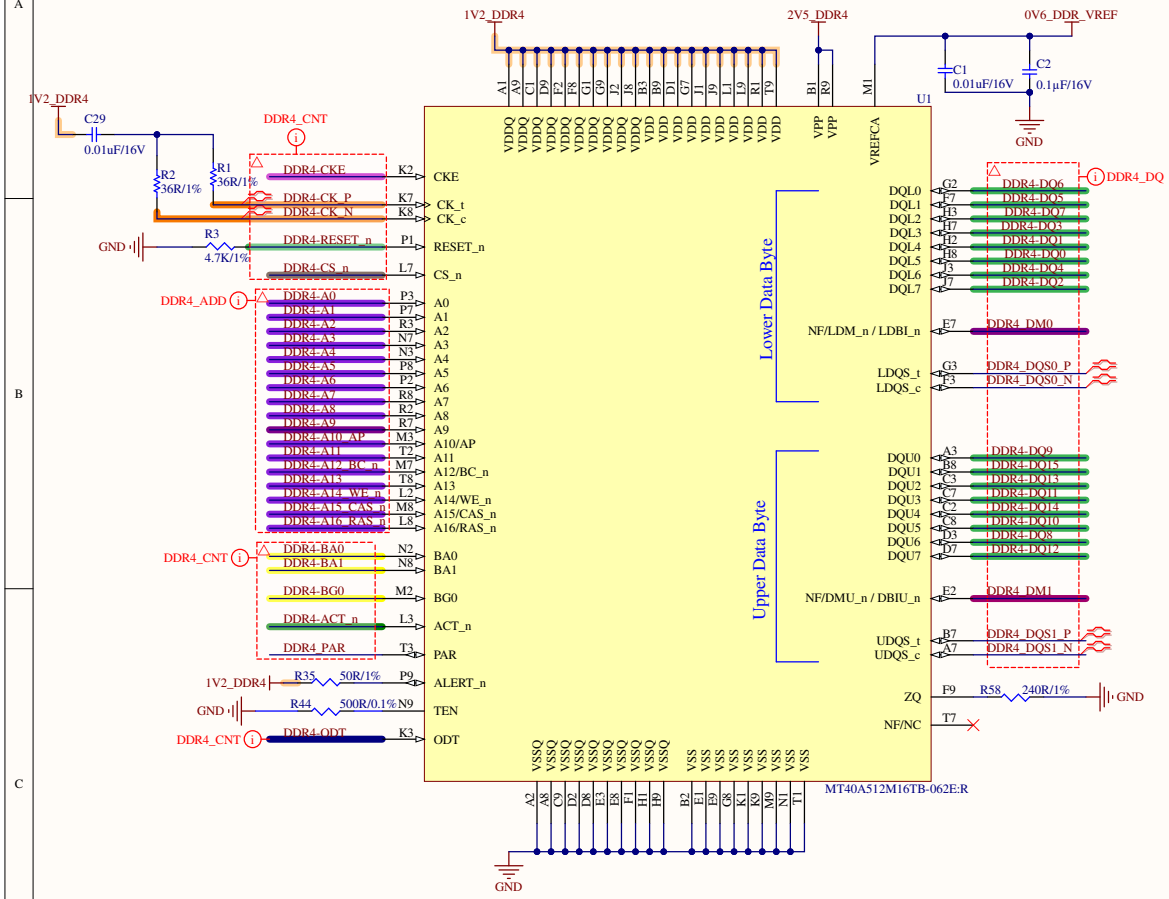
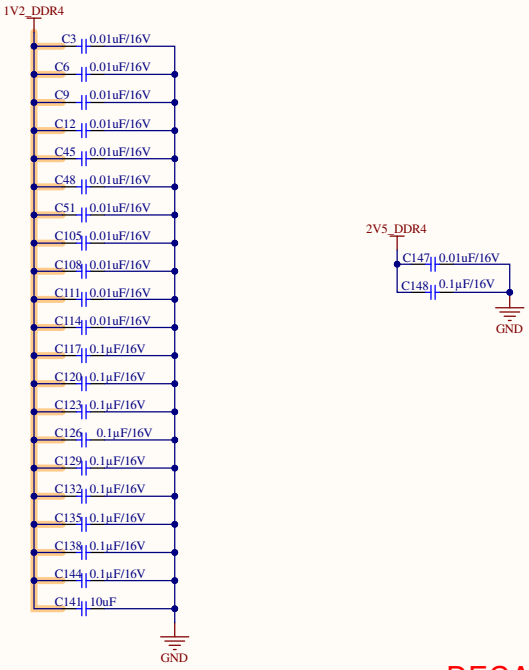
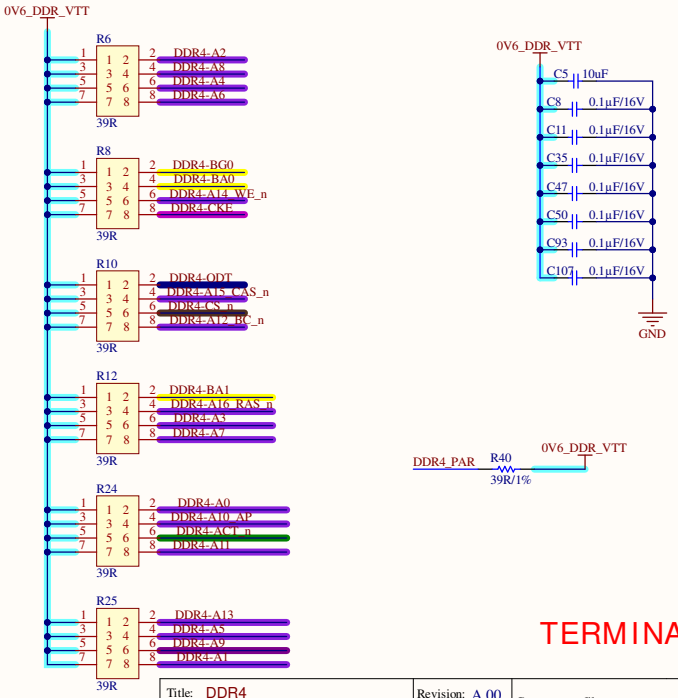
DDR4



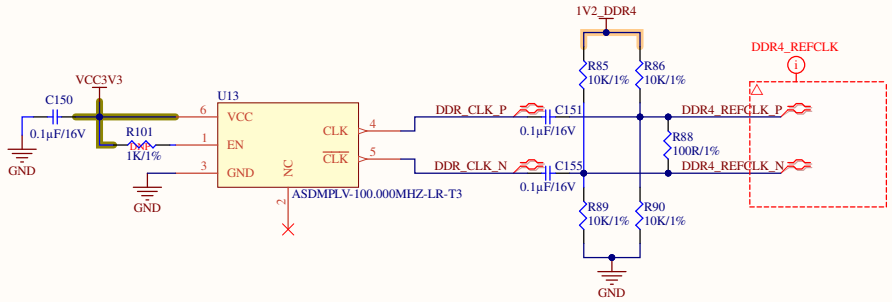
DECAP



TERMINATION



DDR REFERENCE CLOCK 100MHz



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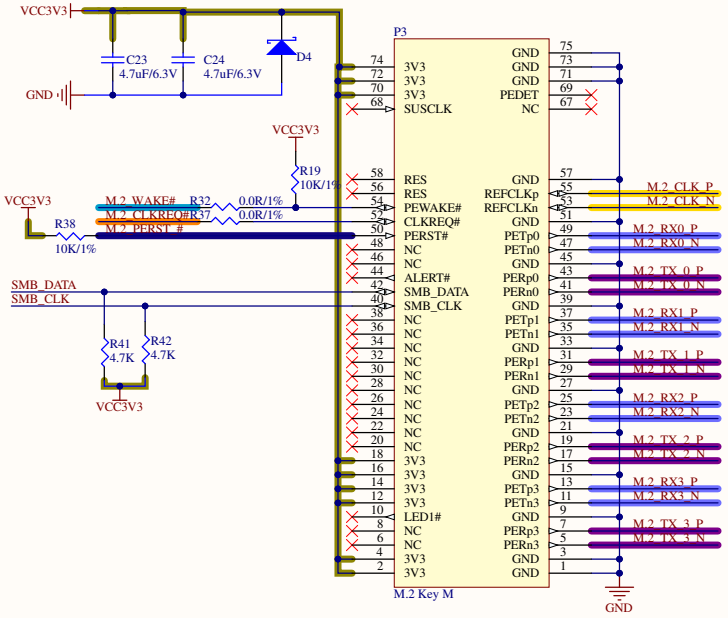
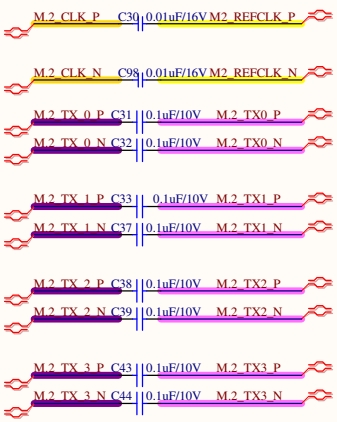
File: DDR4.SchDoc			

M.2





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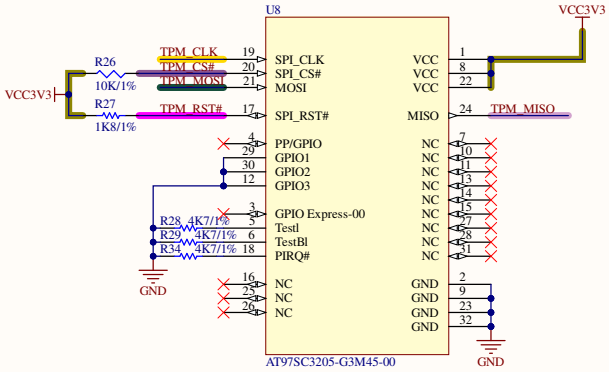

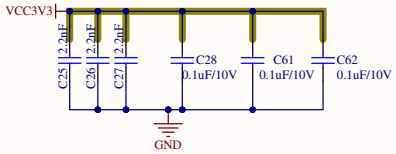

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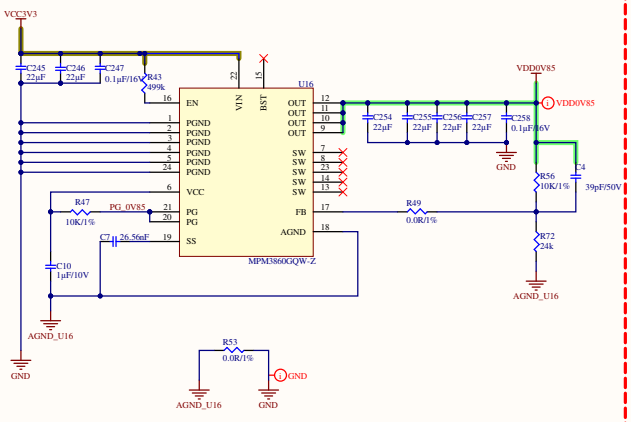
Size: A3	Project: Aller AU Plus.PrjPcb		
Date: 12-03-2025	Time: 10:04:46	Sheet 4 of 7	
File: M.2.SchDoc			

POWER VCC0V85 (VCCINT)



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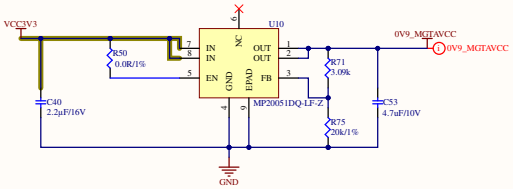
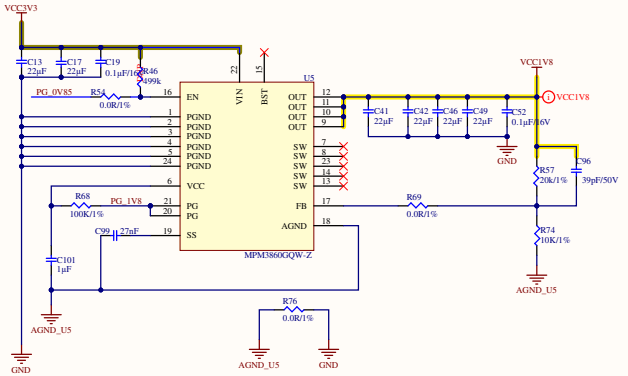
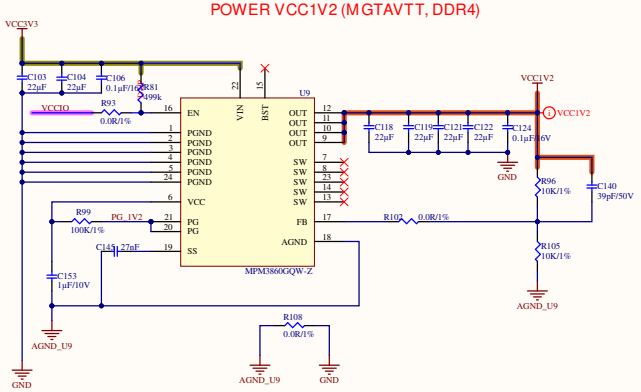


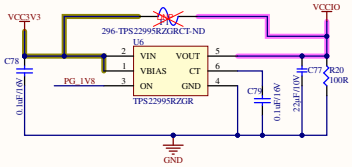
POWER VCC1V8 (VCCAUX, VCCO)



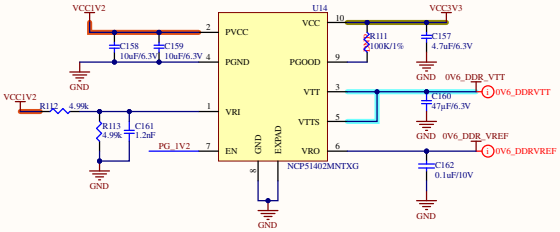
POWER VCC1V2 (MGTAVTT, DDR4)



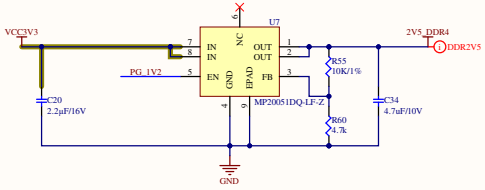
POWER VCCIO 3V3



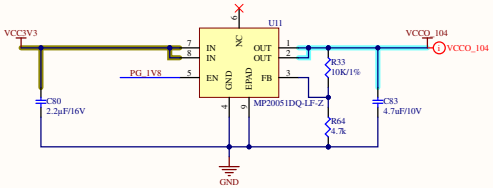
DDR4 0V6 (VTT/VREF)



POWER 2V5 (DDR4 VPP)



POWER VCCIO 2V5



P4 FD 1mm FUDIUAL

P5 FD 1mm FUDIUAL

P6 FD 1mm FUDIUAL

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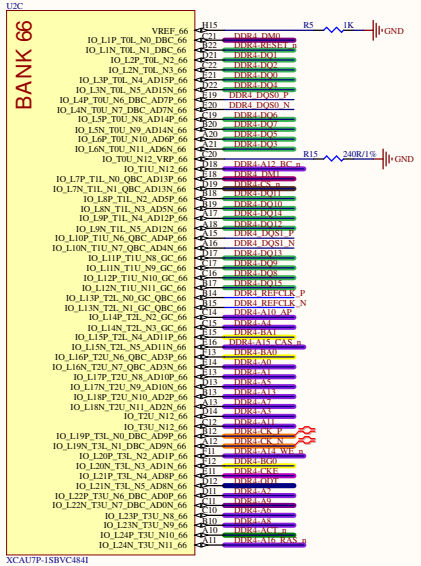
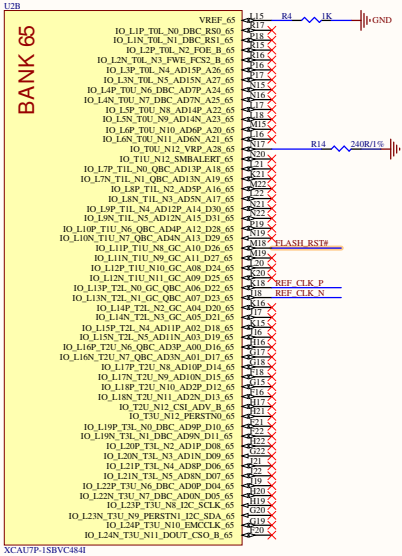
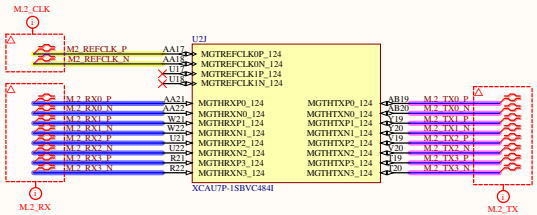
Date: 12-03-2025	Time: 10:04:47	Sheet 5 of 7	
File: Power Supply.SchDoc			

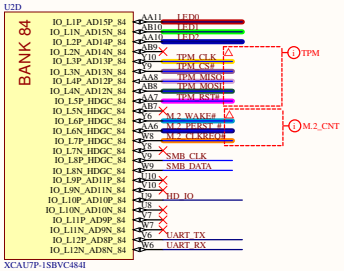
HP BANKS

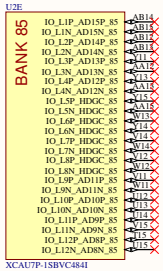


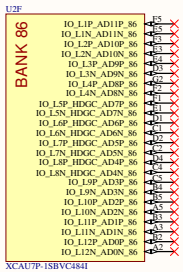


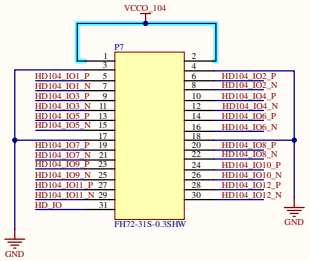
GTH BANK 124

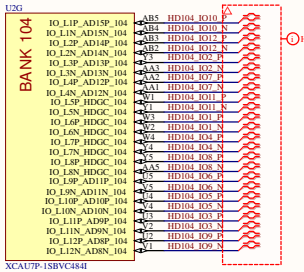


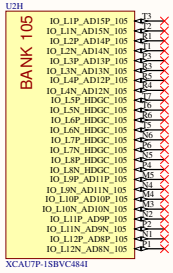


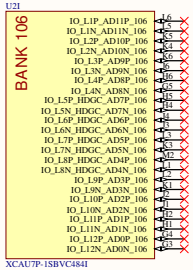












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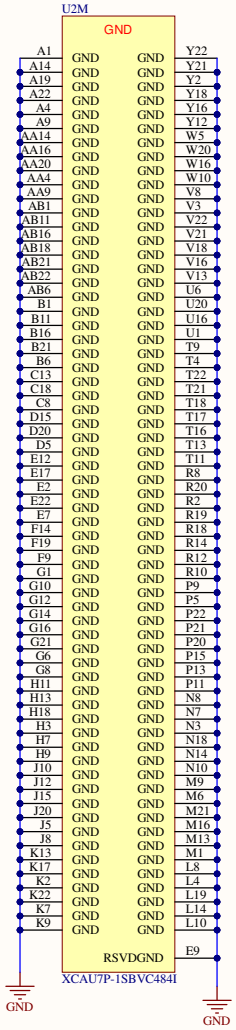
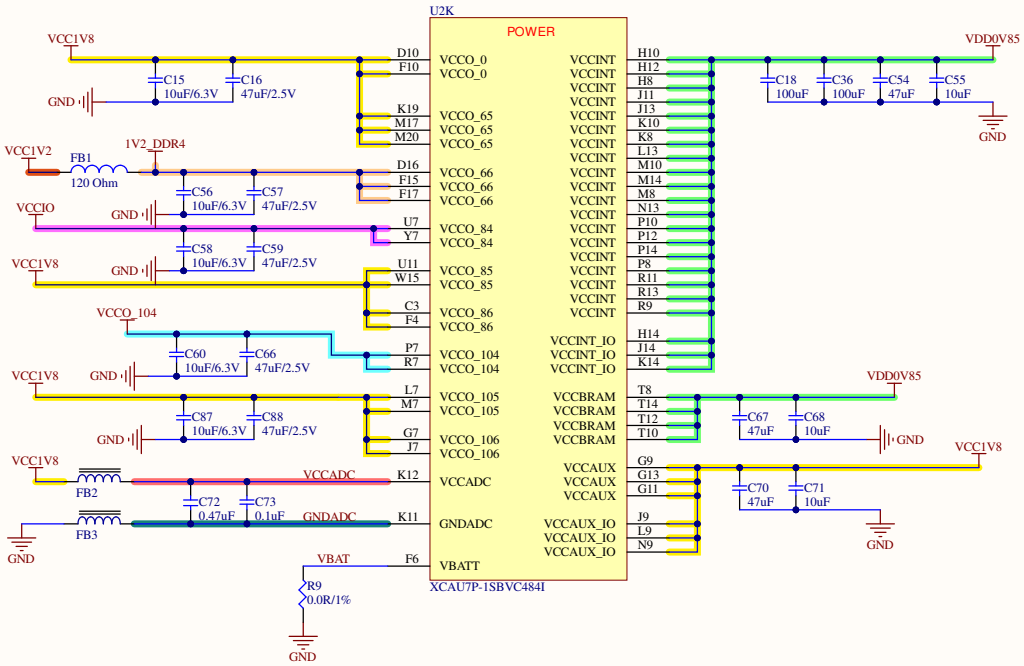
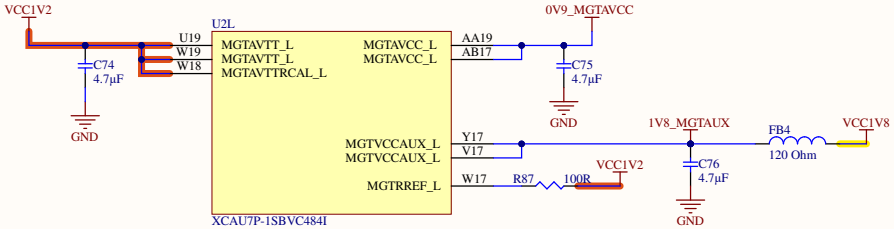
File: FPGA_A.SchDoc		

FPGA POWER







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File: FPGA_PWR.SchDoc			