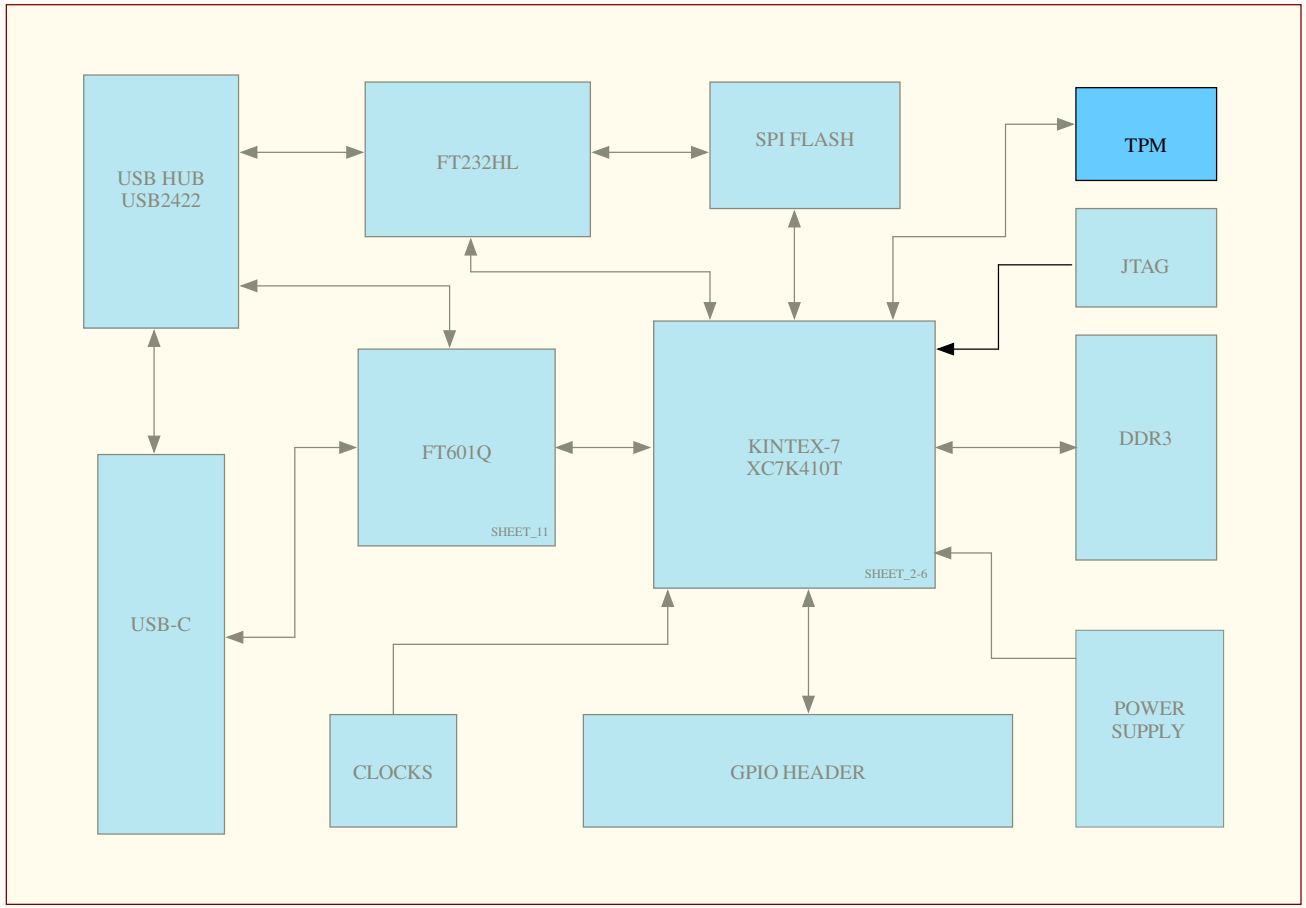
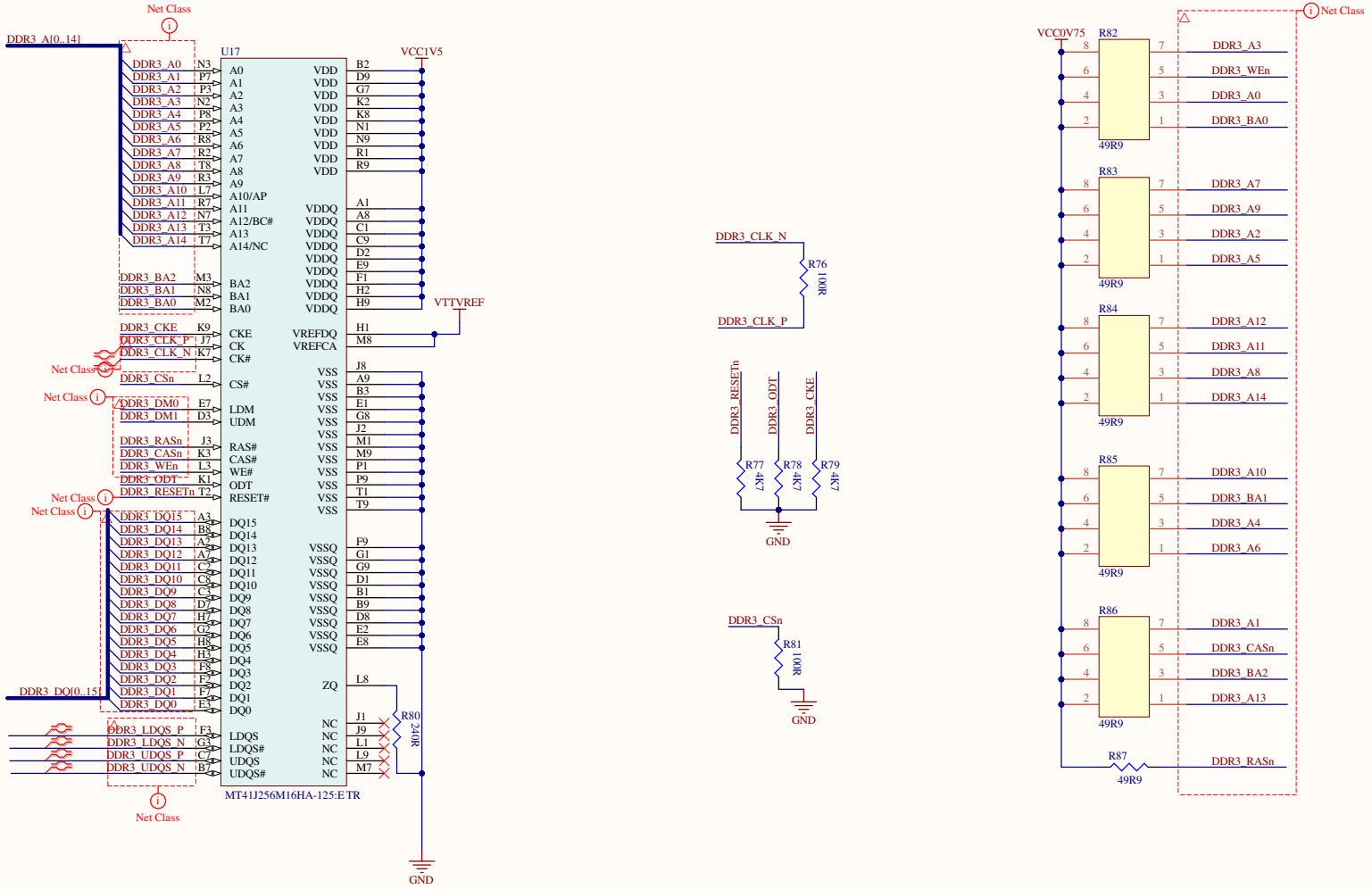
Block Diagram

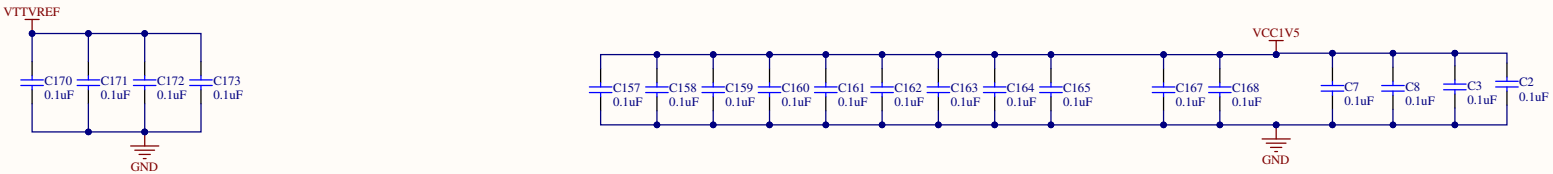
CALLISTO-K7



Title: Block Diagram		Revision: V2.0	Numato Lab
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:52:57	Sheet 1 of 11	
File: Sheet1.SchDoc			

DDR3

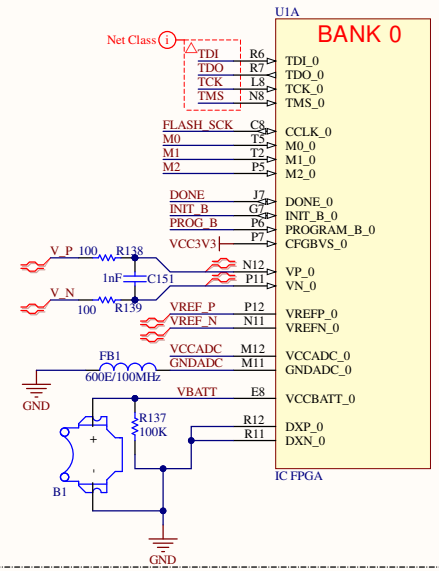




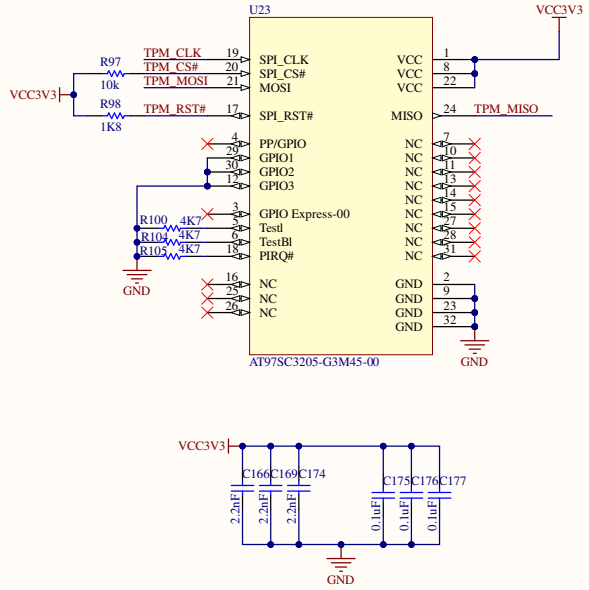
Title: DDR3		Revision: V2.0	
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:52:57	Sheet 2 of 11	
File: Sheet2.SchDoc			

NumatoLab

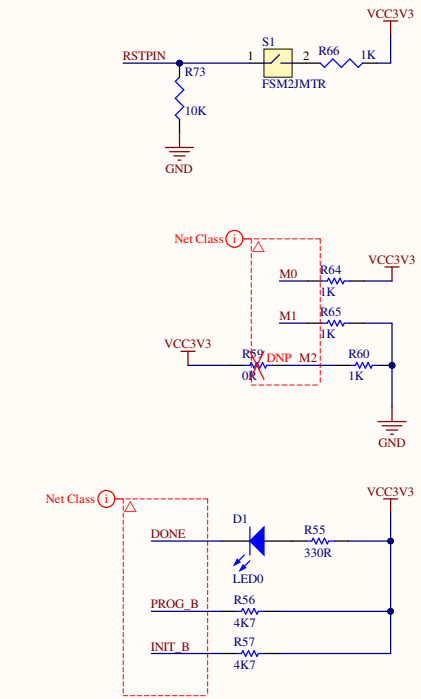
FPGA Bank0



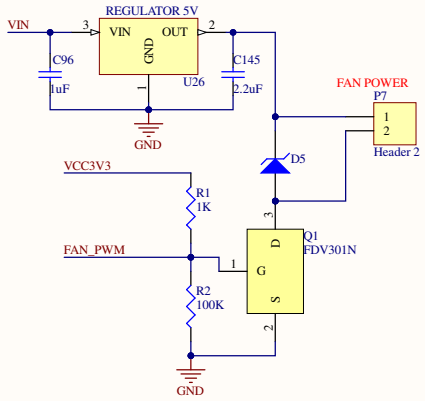
TPM



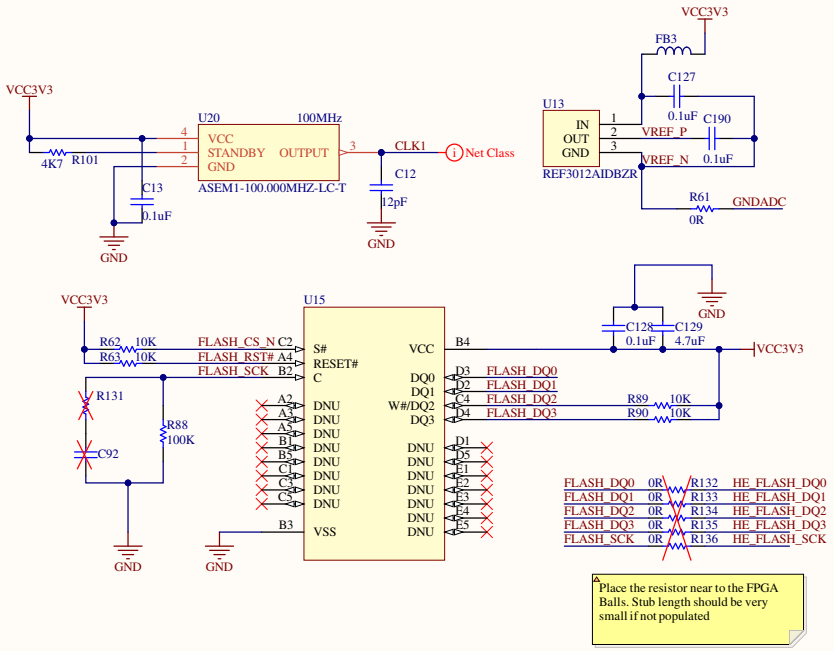
FPGA Configuration



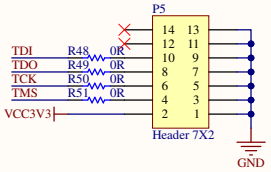
FAN Power



Clock, ADC Reference and Flash



JTAG

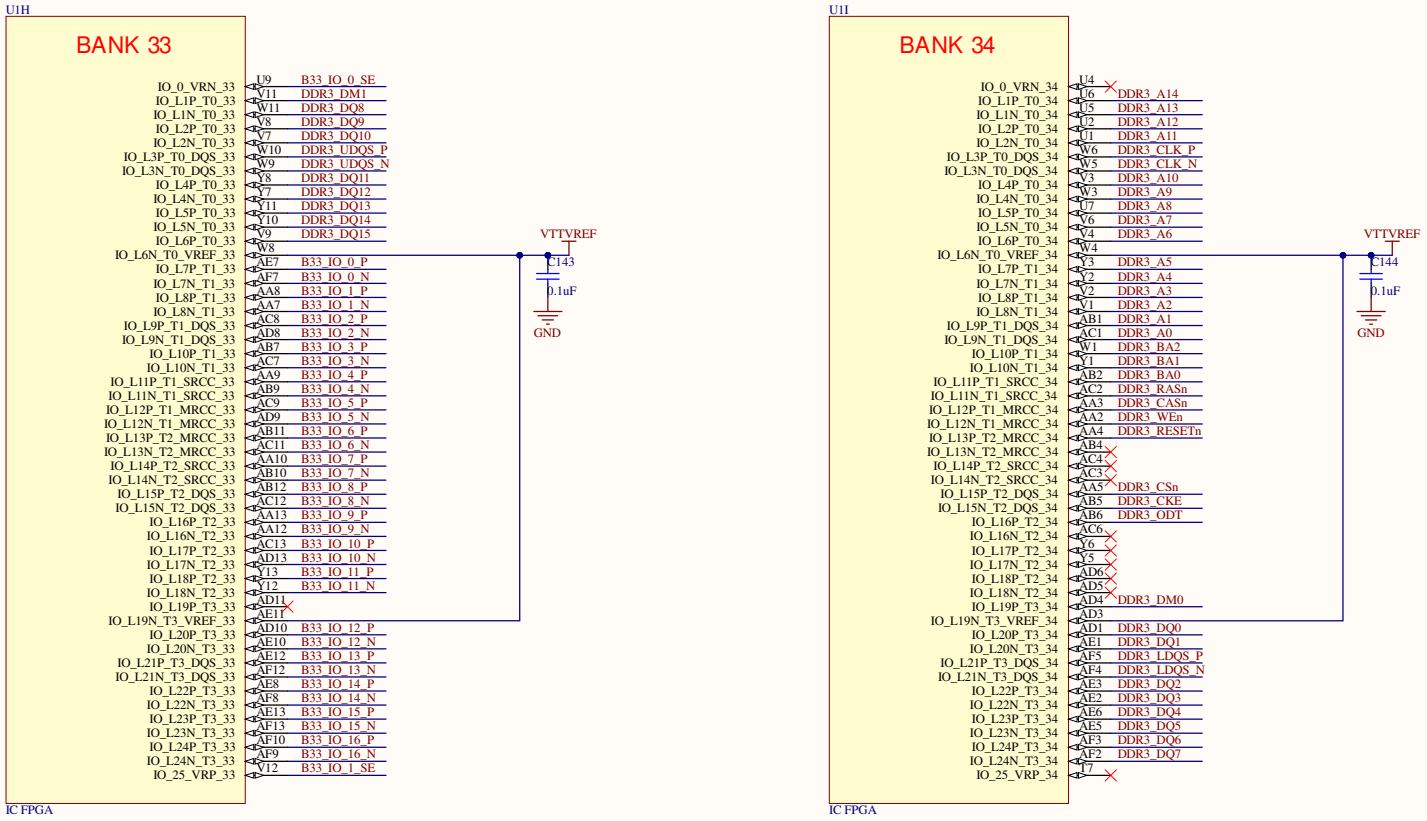


FPGA Configuration

Title: FPGA Configuration		Revision: V2.0	
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:52:57	Sheet 3 of 11	
File: Sheet3.SchDoc			

Numato Lab

FPGA Banks 33& 34



Title: BANK 33 & 34		Revision: V2.0	
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:52:58	Sheet 4 of 11	
File: Sheet4.SchDoc			

Numato Lab

FPGA Banks 12,13& 14

Title: BANK 12,13,14		Revision: V2.0	
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:52:58	Sheet 5 of 11	
File: Sheet5.SchDoc			

Numato Lab

FPGA Banks 15,16& 32

ADC filter

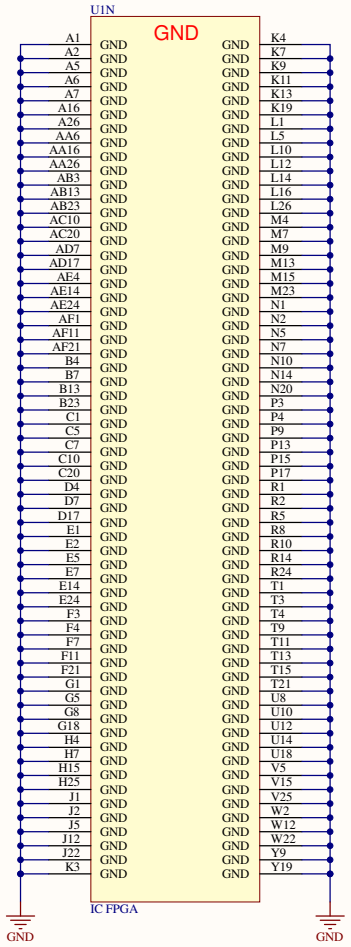
If external analog inputs are not used all these resistors should be 0R and all these capacitors should be DNP.

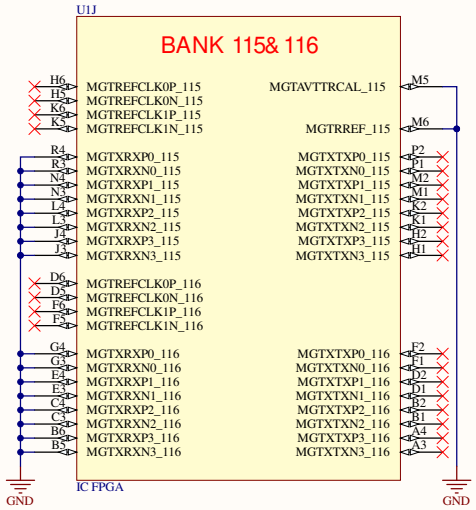
Title: BANK 15, 16, 32		Revision: V2.0	
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:52:59	Sheet 6 of 11	
File: Sheet6.SchDoc			

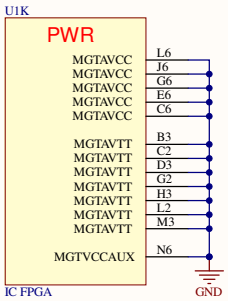
Numato Lab

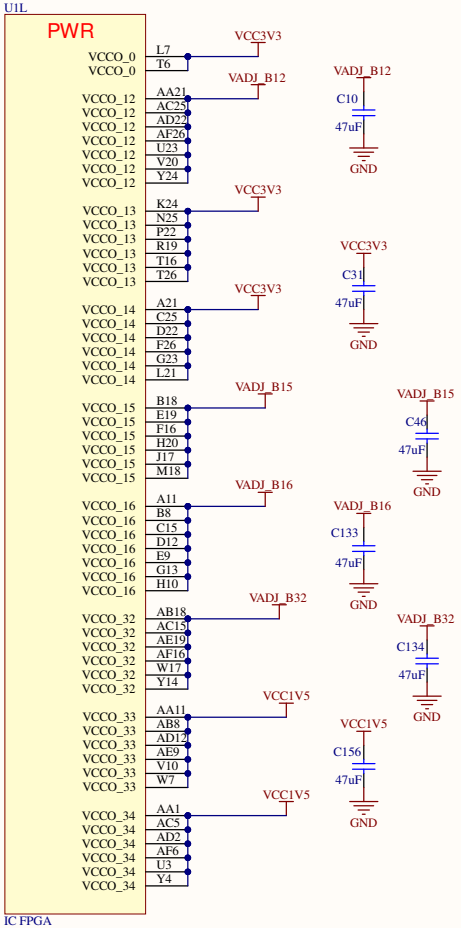
FPGA GND

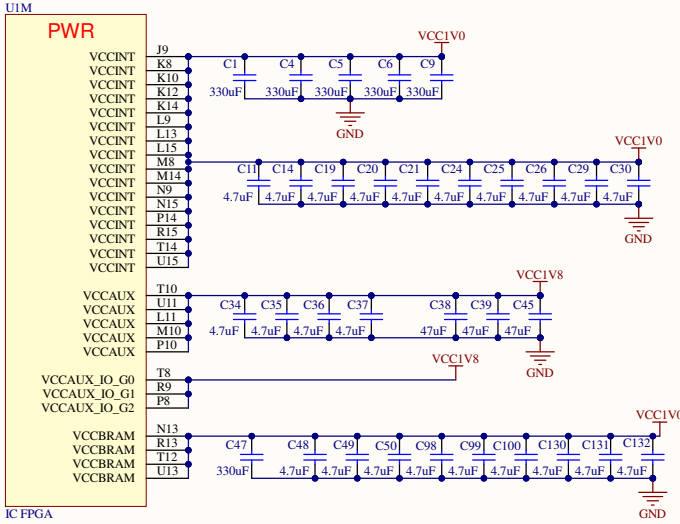
FPGA GTX & Power



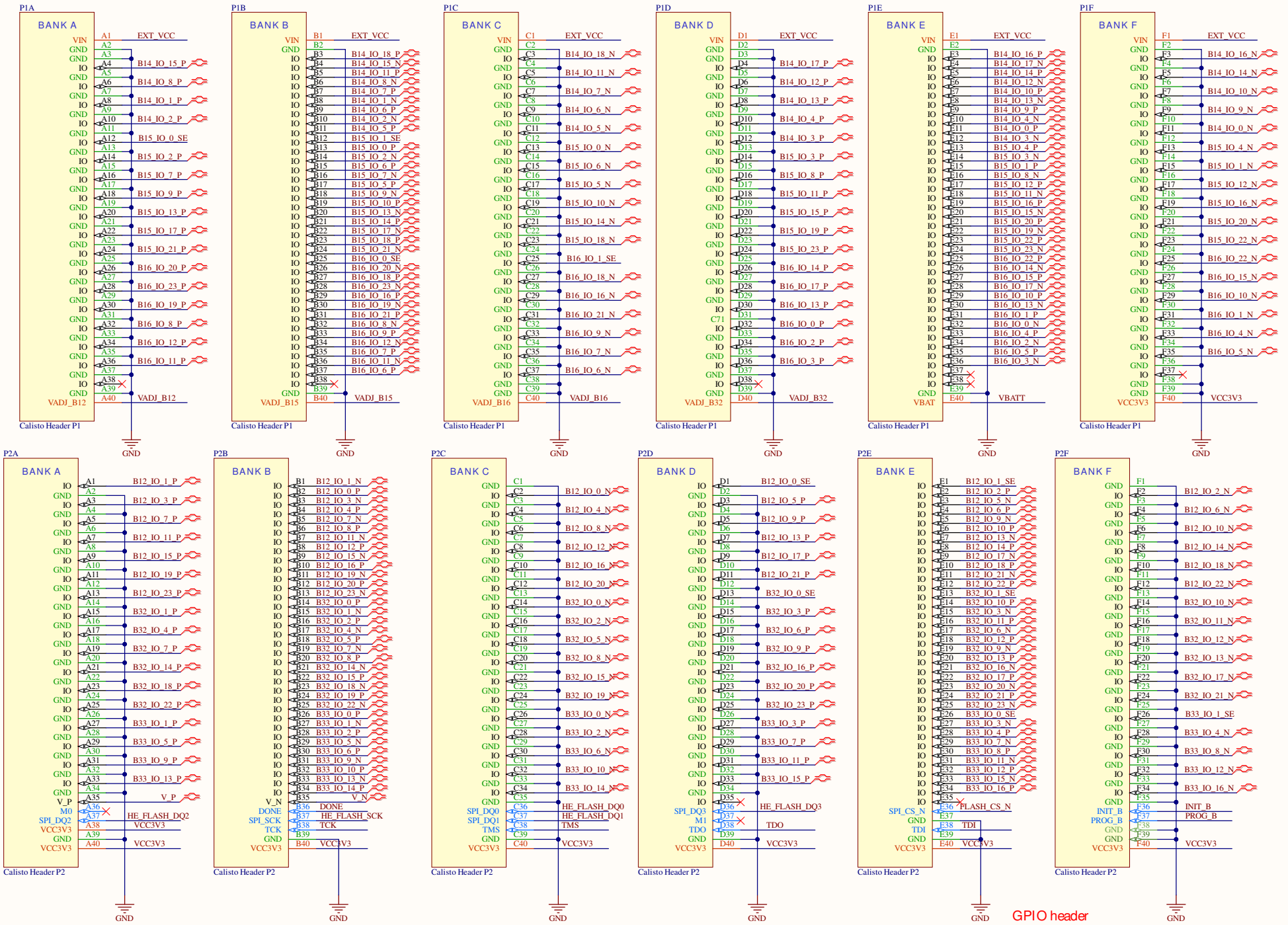






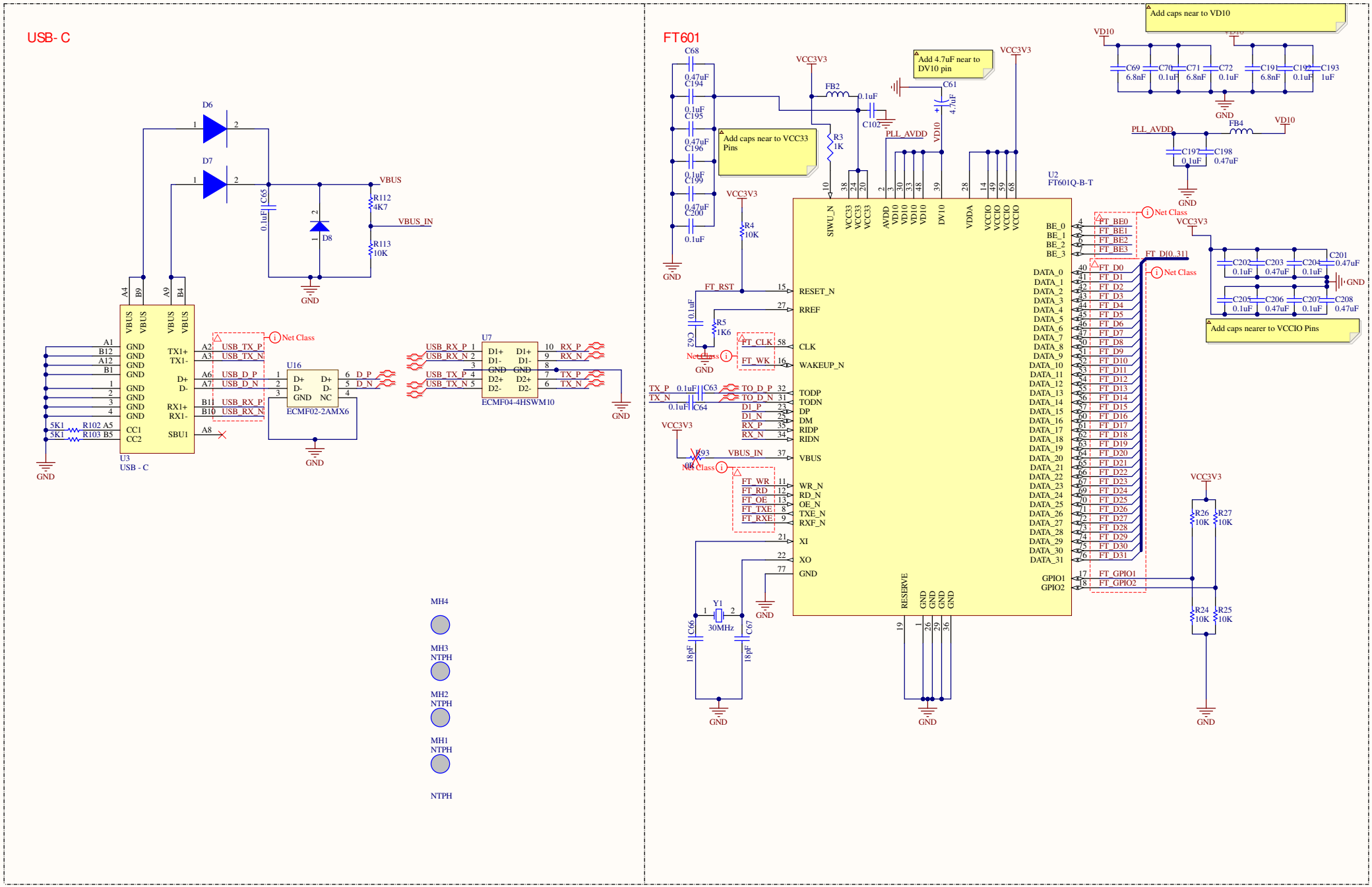


Title: FPGA POWER & GND		Revision: V2.0	Numato Lab
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:52:59	Sheet 7 of 11	
File: Sheet7.SchDoc			



Title: GPIO		Revision: V2.0	
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:53:00	Sheet 8 of 11	
File: Sheet8.SchDoc			

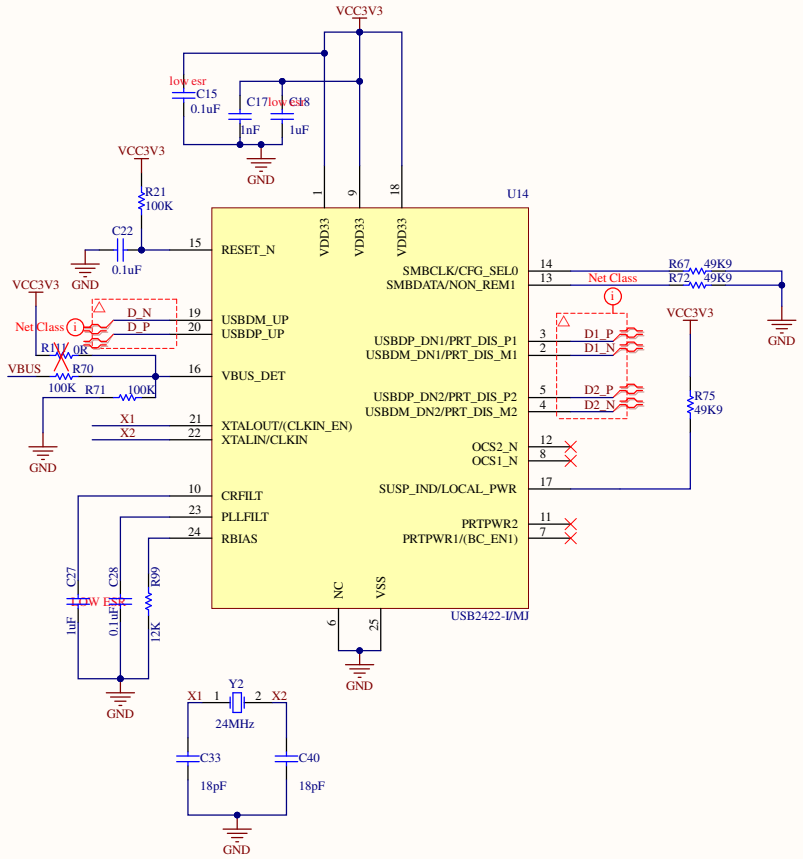
Numato Lab



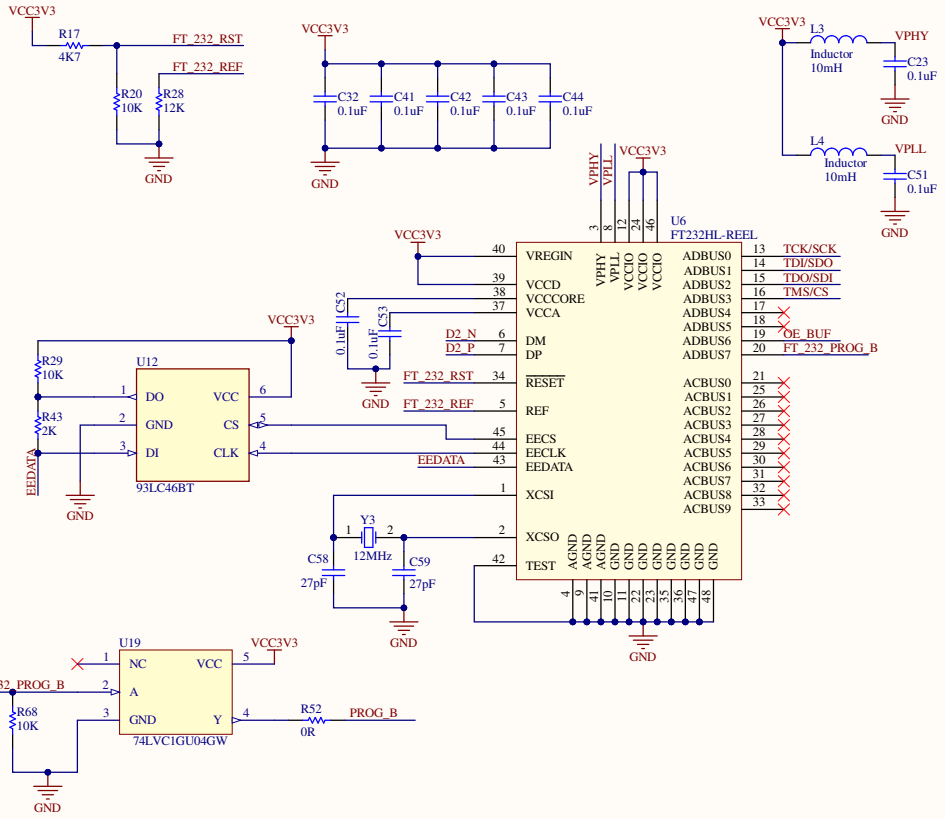
Title: USB		Revision: V2.0	
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:53:00	Sheet 9 of 11	
File: Sheet9.SchDoc			

Numato Lab

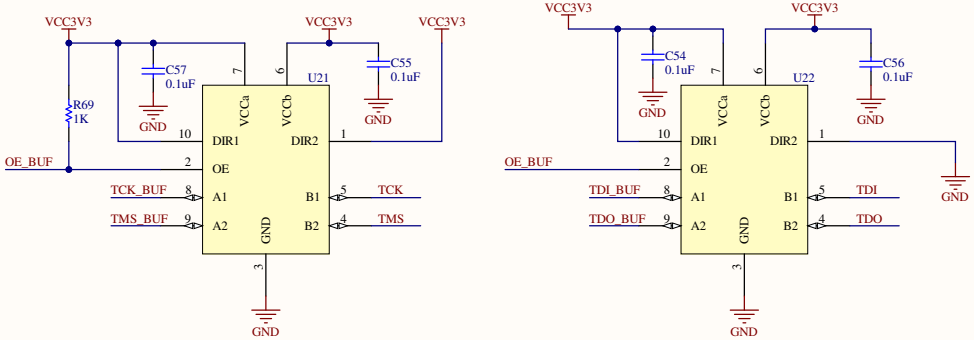
USB2422

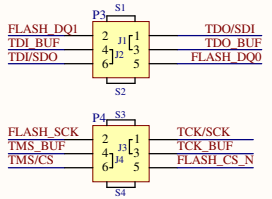


FT232



Buffer

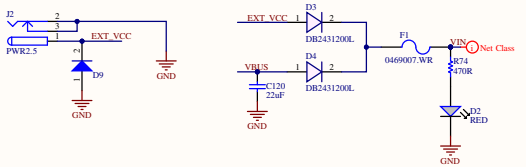




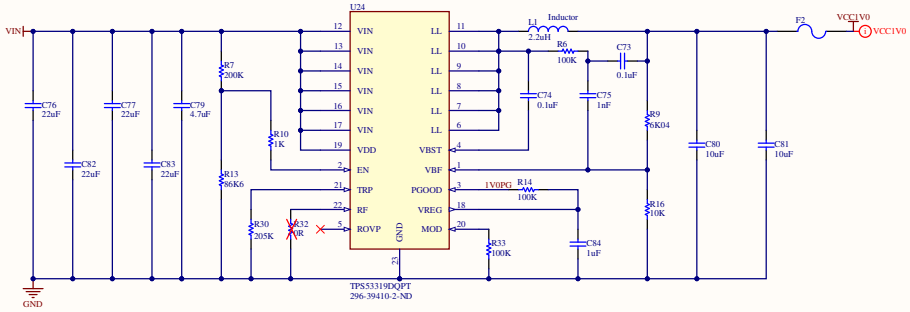
Jumper on - J1,J2,J3,J4 - JTAG COMMUNICATION
Jumper on - S1,S2,S3,S4 - SPI COMMUNICATION

Title: HUB		Revision: V2.0	NumatoLab
Size: A3	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:53:00	Sheet 10 of 11	
File: Sheet10.SchDoc			

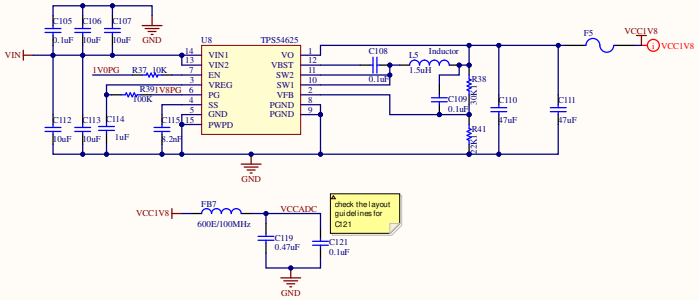
Power Input



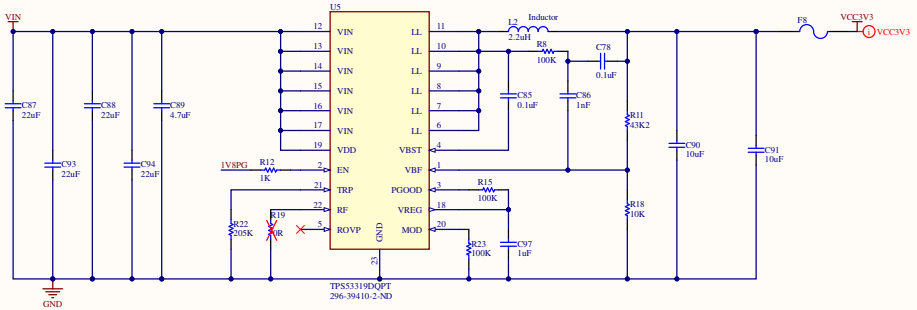
12V0 to 1V0



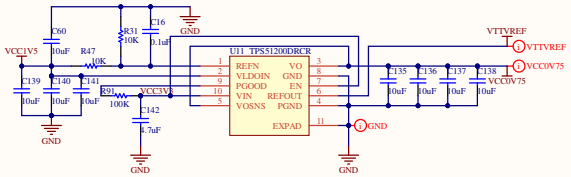
12V0 to 1V8



12V0 to 3V3

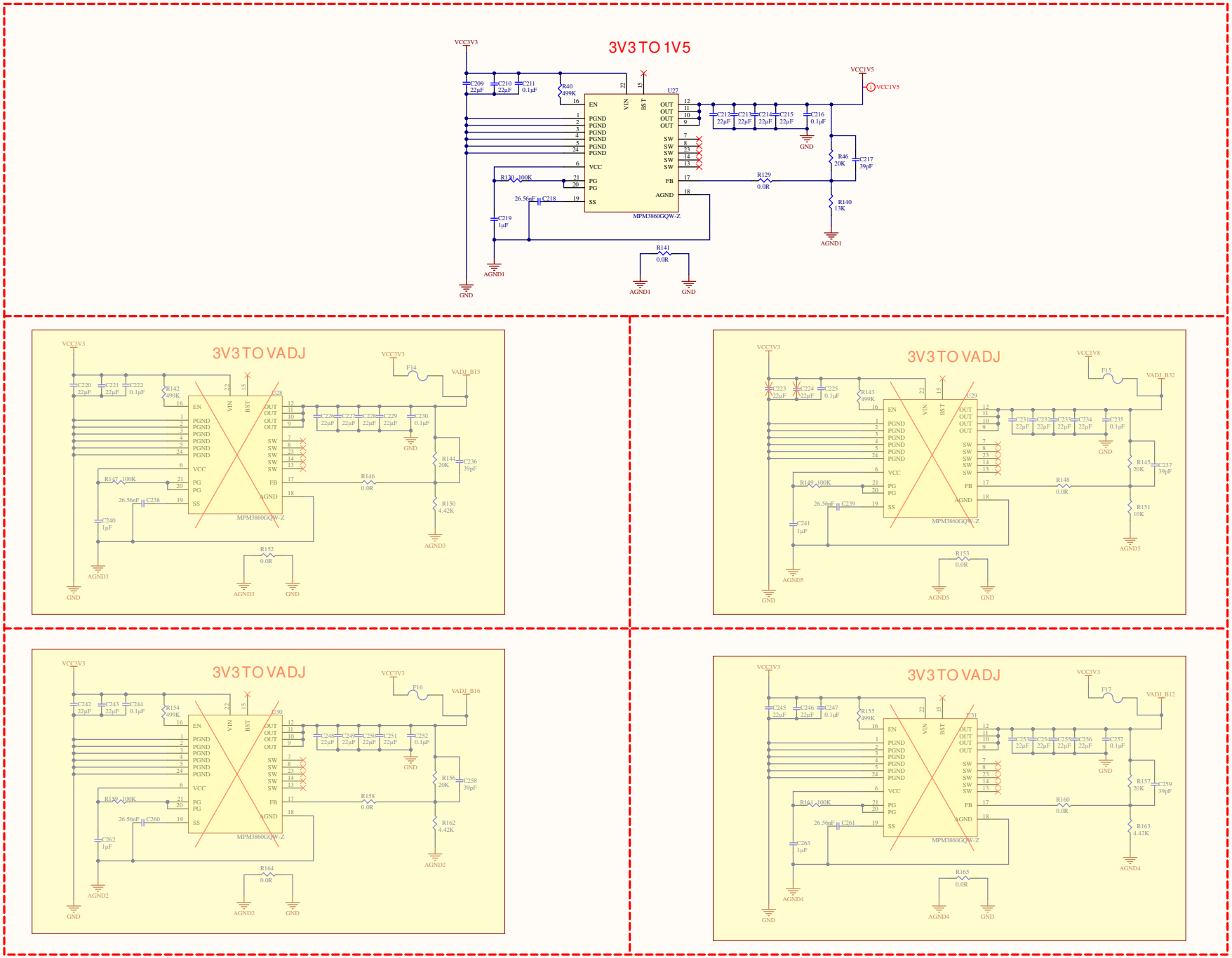


DDR Reference



Title: POWER SUPPLY		Revision: V2.0	
Size: A2	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:53:01	Sheet 11 of 11	
File: Sheet11.SchDoc			

Numato Lab



Title: Pwr_supply		Revision: V2.0	Numato Lab
Size: A2	Project: CallistoK7.PrjPcb		
Date: 27-07-2023	Time: 09:53:01	Sheet * of *	
File: Pwr_supply.SchDoc			