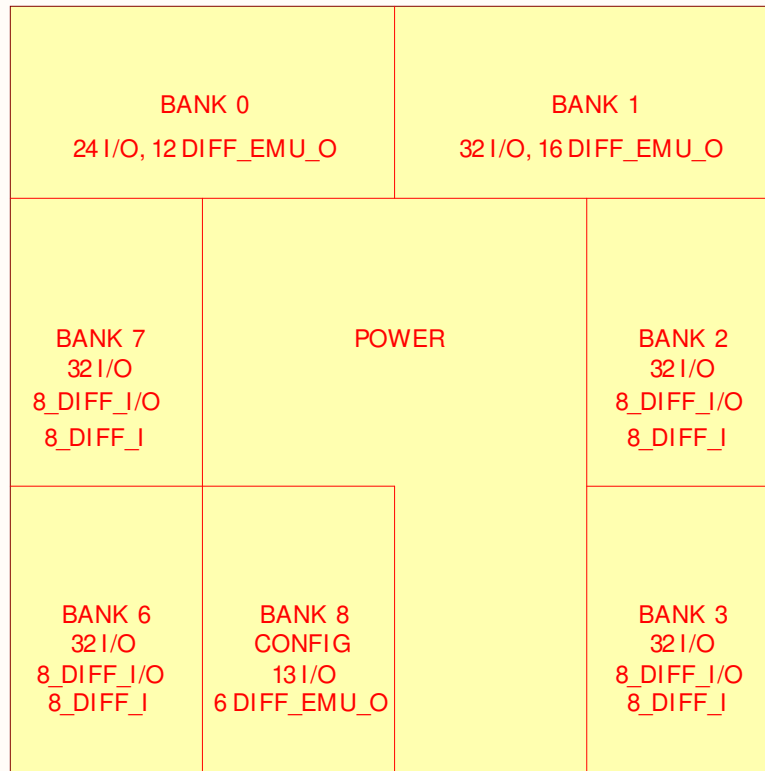


LFE5U-45F-7BG256I IO MAP



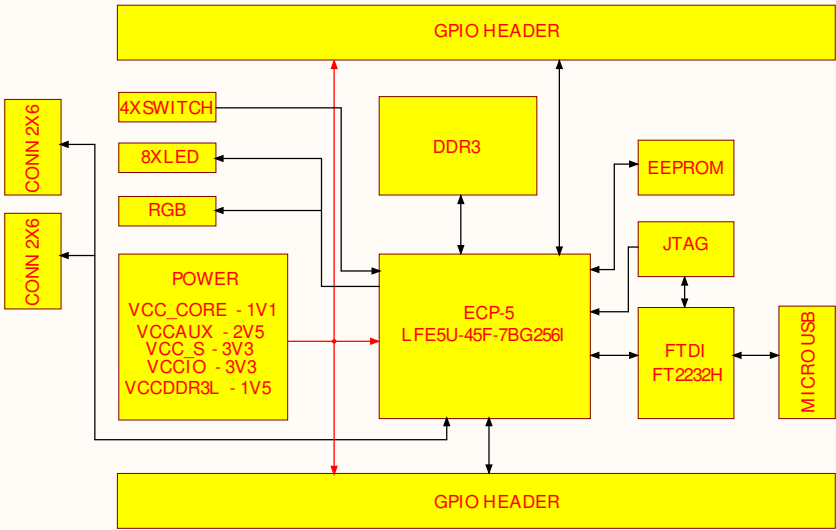
IO PLANNING:

LPDDR3 : BANK 7, BANK 6
 CONFIG, LED, SWITCH : BANK 8, BANK 0
 IO HEADER : BANK 1, BANK 2, BANK 3

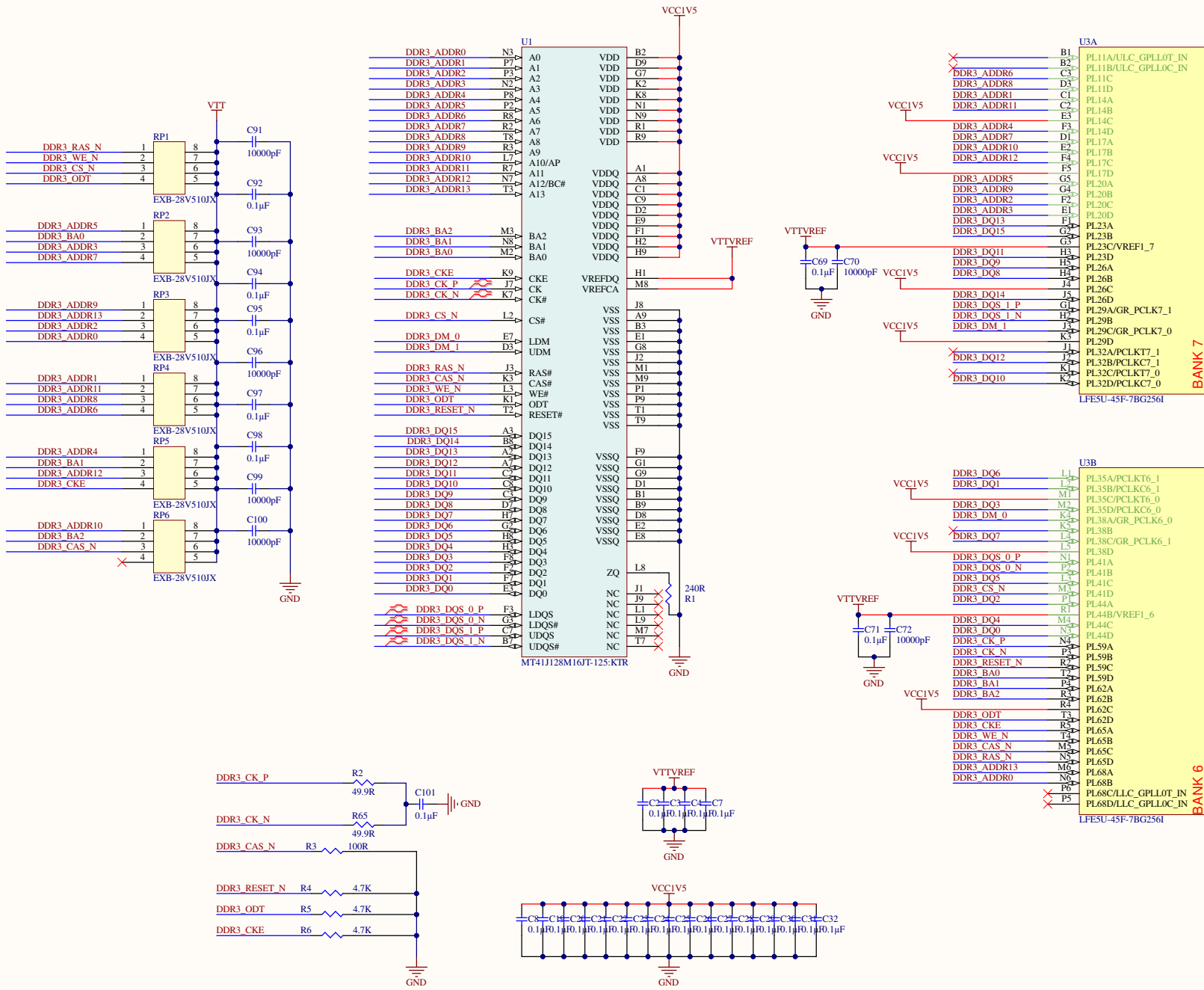
NOTE:

I/O : Single ended I/O
 DIFF_EMU_O : Differential_emulated_output
 DIFF_I/O : Differential_I/O
 DIFF_I : Differential_Input

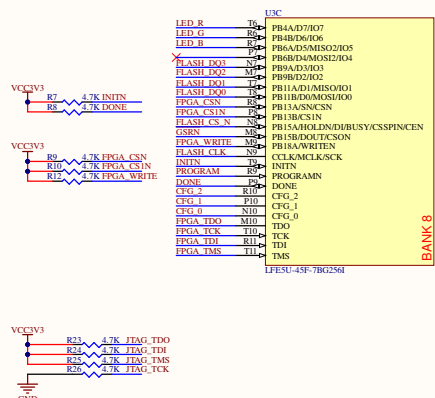
BLOCK DIAGRAM



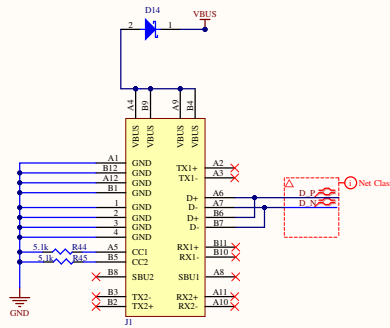
DDR3_FPGA



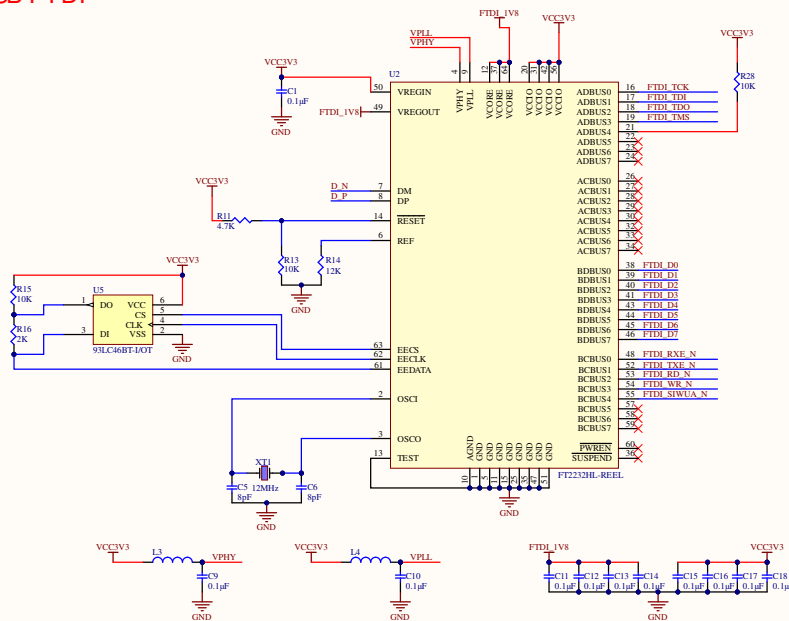
FPGA CONFIG



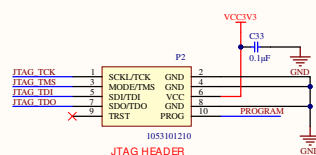
USB



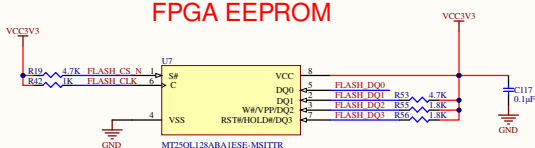
USB FTDI



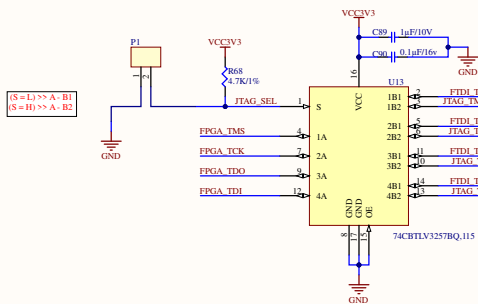
FPGA JTAG



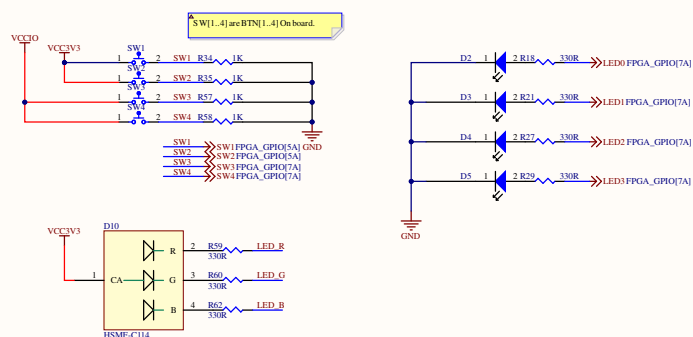
FPGA EEPROM



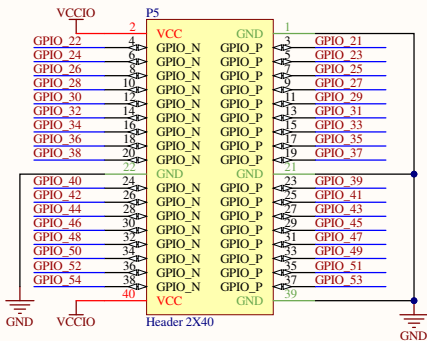
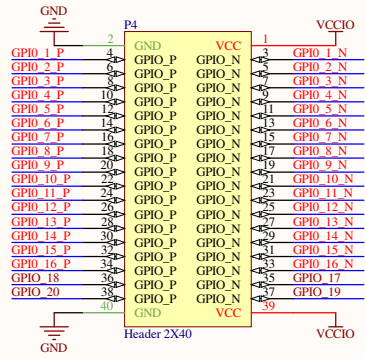
FPGA JTAG BUFFER



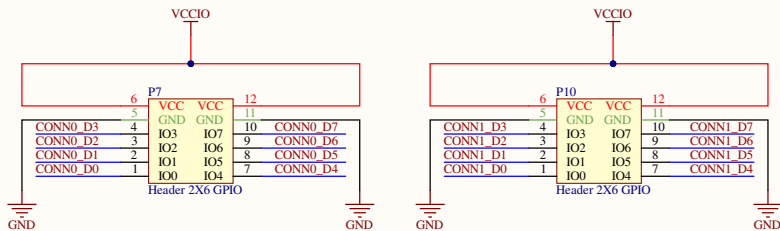
LED & SWITCHES



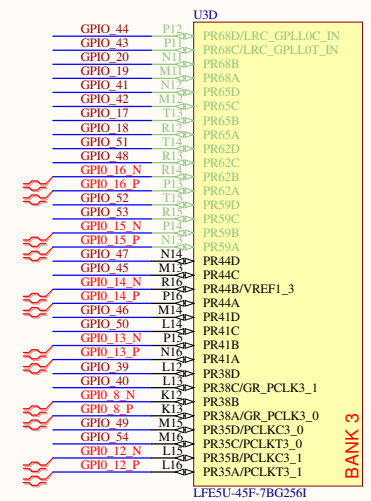
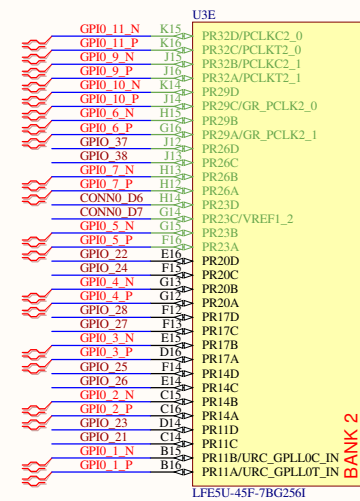
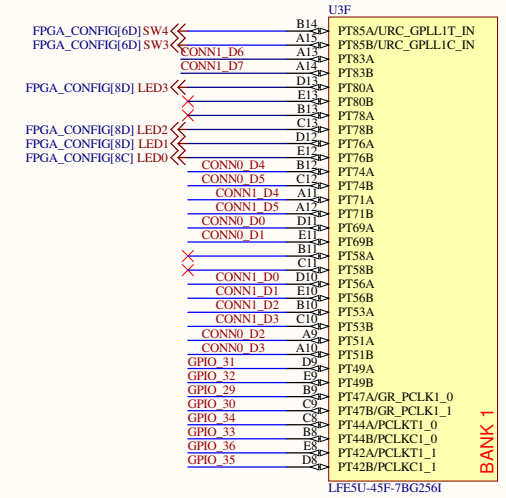
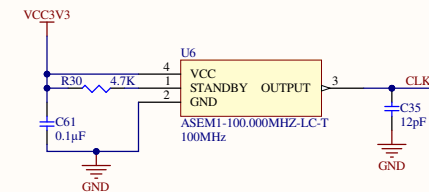
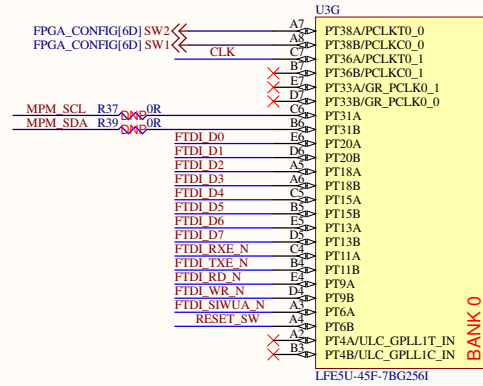
CONNECTOR GPIO



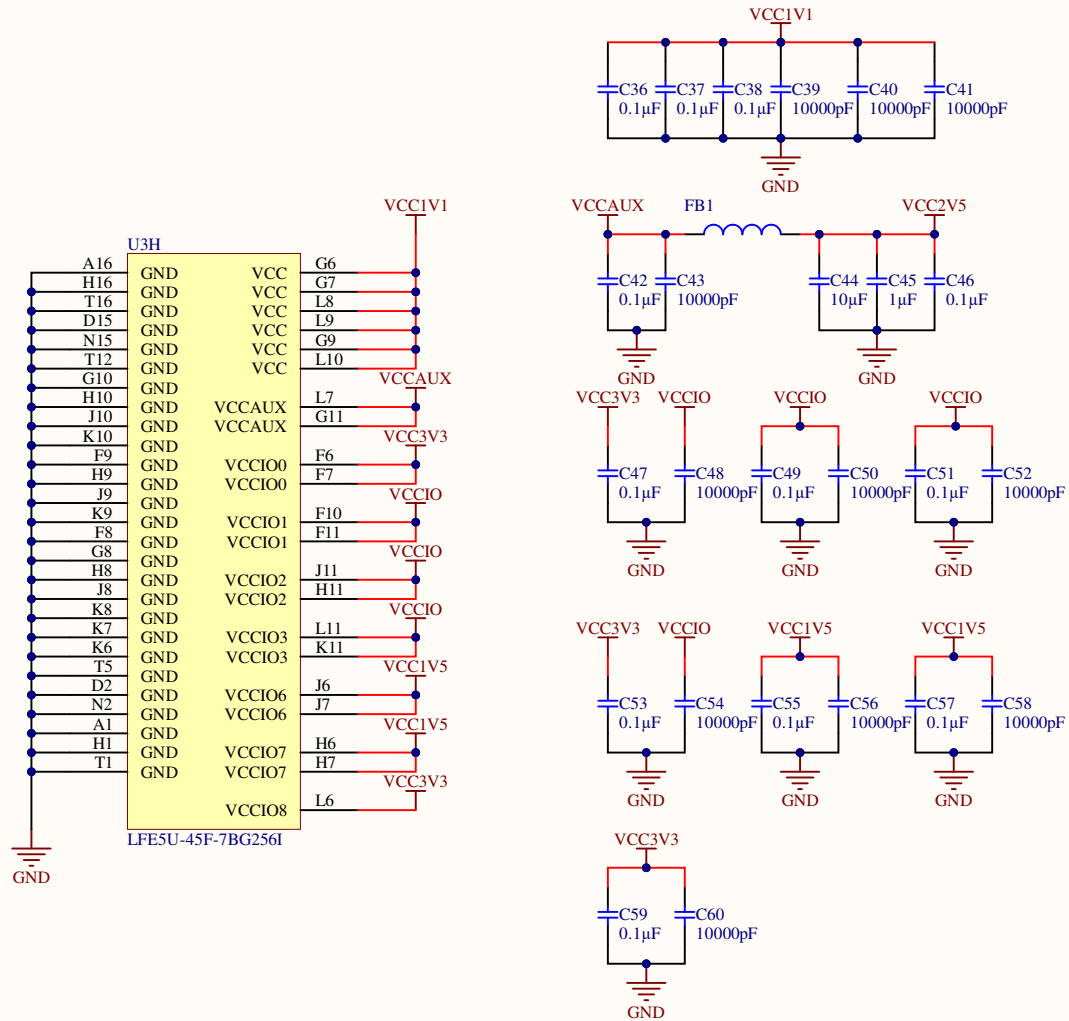
GPIO 2X6 CONNECTOR



FPGA GPIO



FPGA POWER



Title: FPGA_POWER		Revision: V2.1
Size: A4	Project: Mimas_ECP5_Mini_V2.0.PjPCB	
Date: 05-07-2024	Time: 14:49:19	Sheet 6 of 7
File: FPGA_POWER.SchDoc		



POWER SELECTOR

