
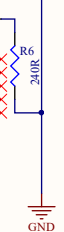
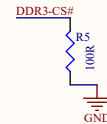
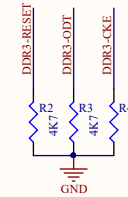
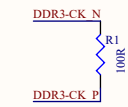
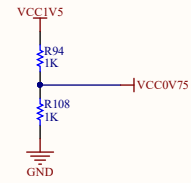
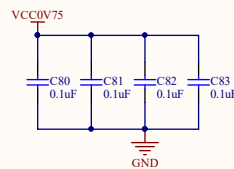
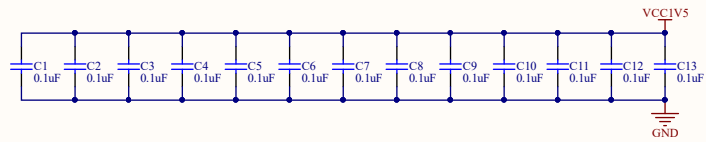
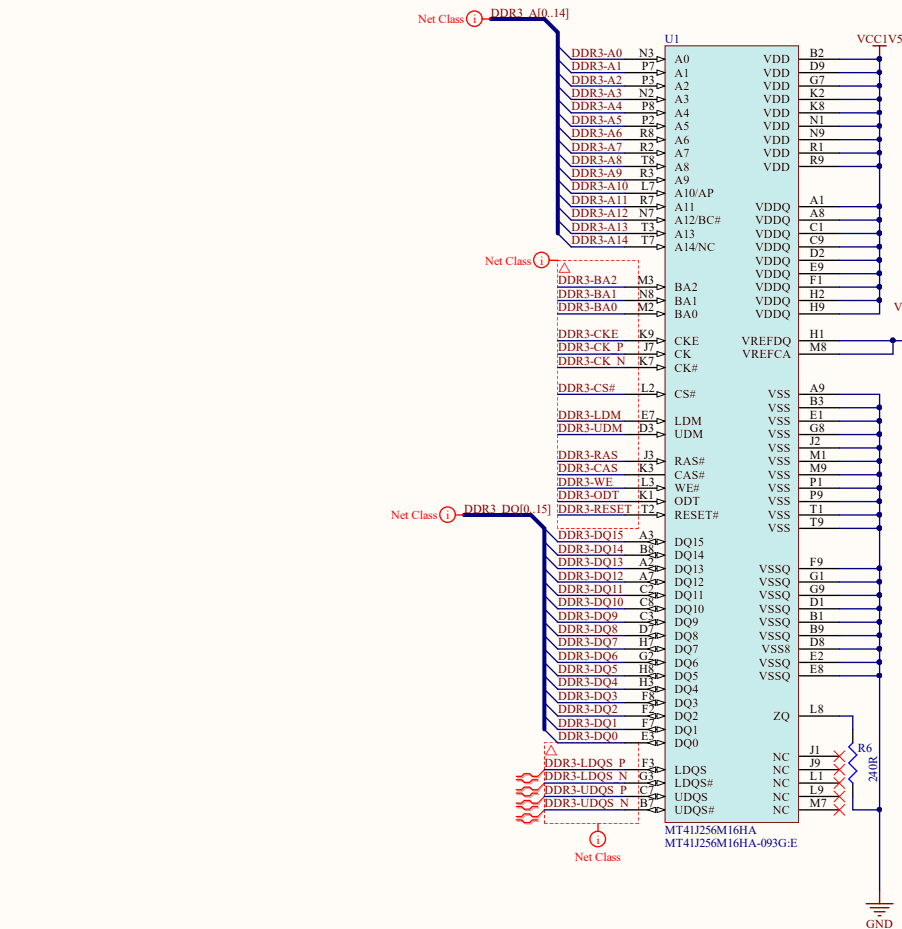



# Block Diagram

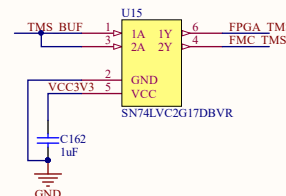
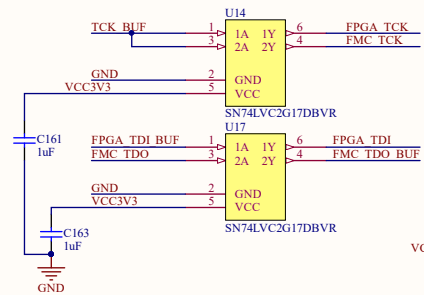
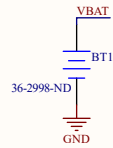
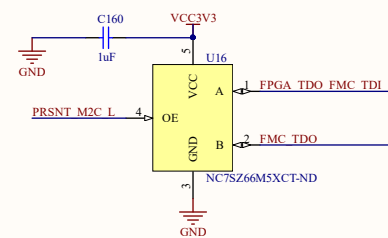
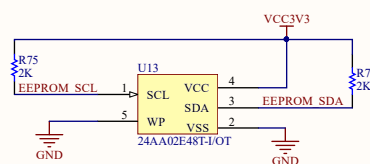
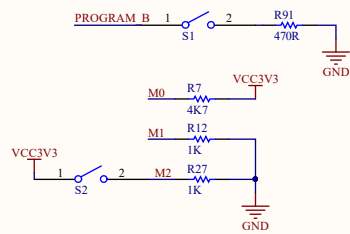
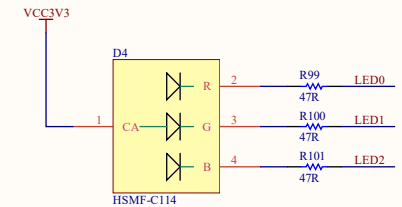
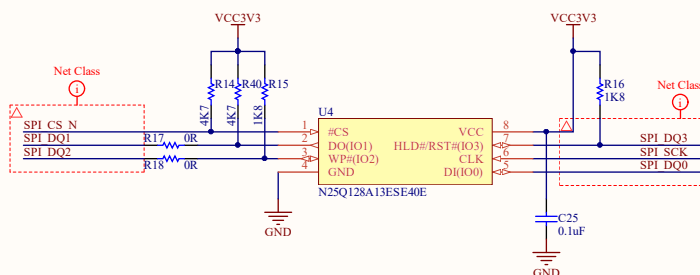
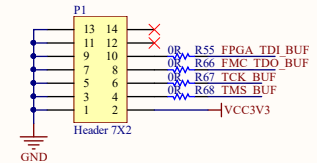
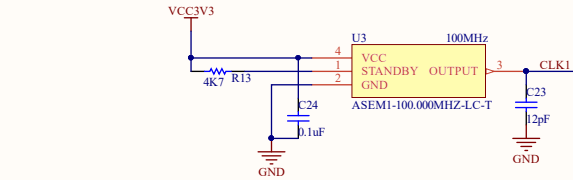
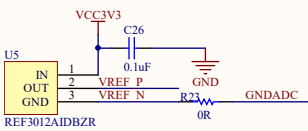
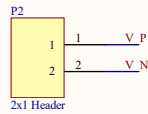
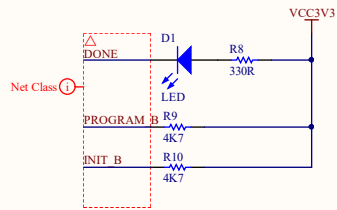
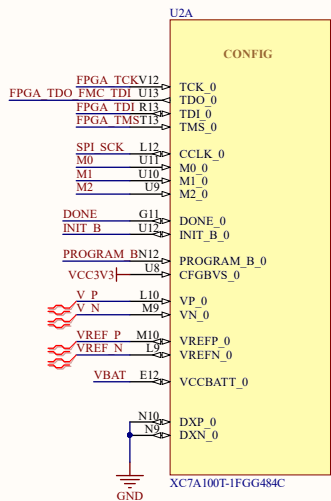
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Size: A3	Project: Tagus.PrjPcb	
Date: 5/2/2018	Time: 17:15 PM	
File: Block Diagram.SchDoc	Sheet 1 of 9	






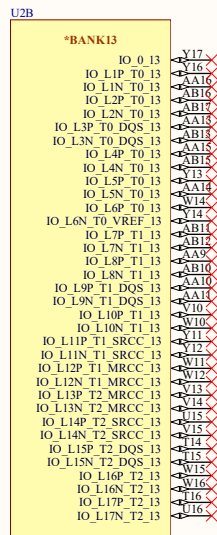
# DDR3

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Date: <b>5/2/2018</b>	Time: <b>17:15 PM</b>		
File: <b>DDR3.SchDoc</b>	Sheet <b>2</b> of <b>9</b>		

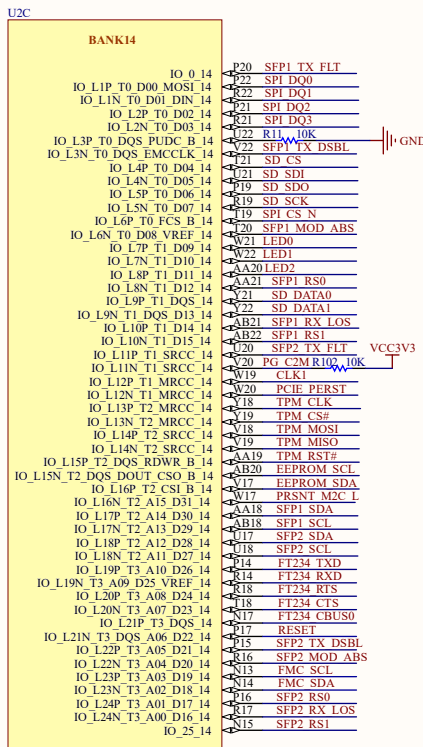


# FPGA Configuration

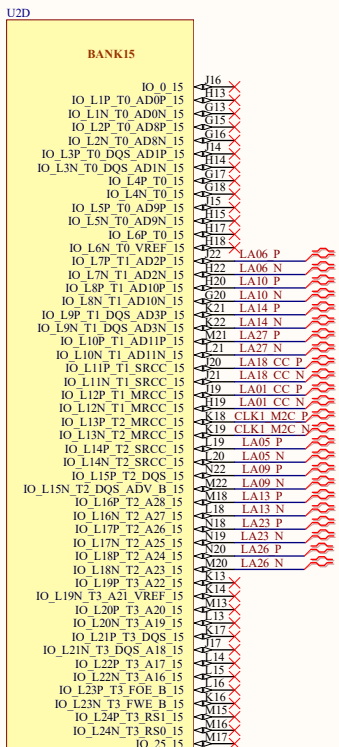
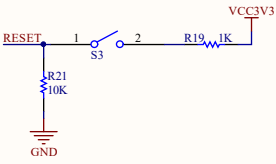
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Size: A3	Project: Tagus.PrgPcb	
Date: 5/2/2018	Time: 17:16 PM	
File: FPGA_C_SchDoc	Sheet 3 of 9	



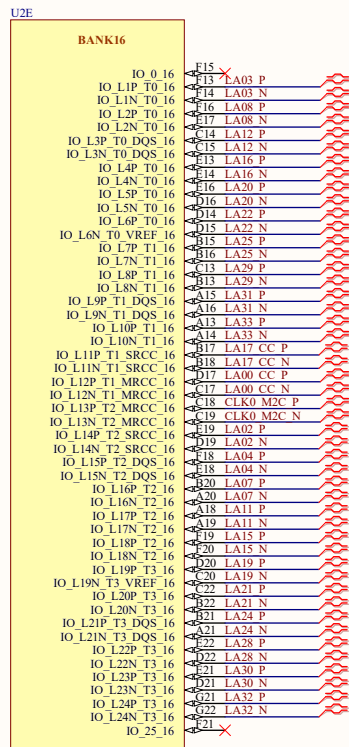
XC7A100T-1FGG484C



XC7A100T-1FGG484C

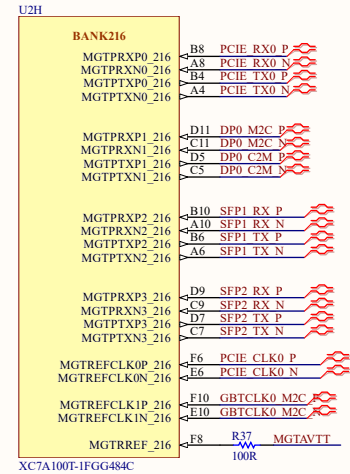
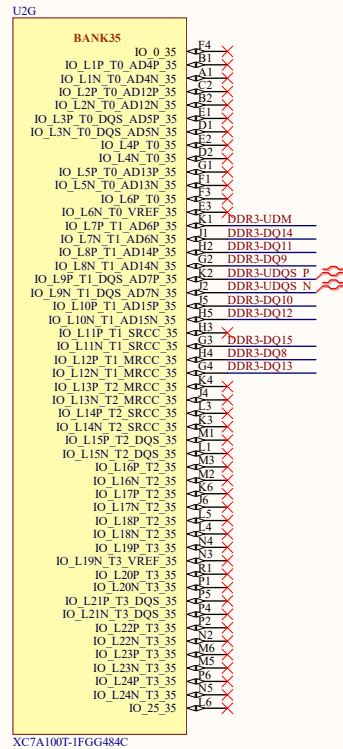
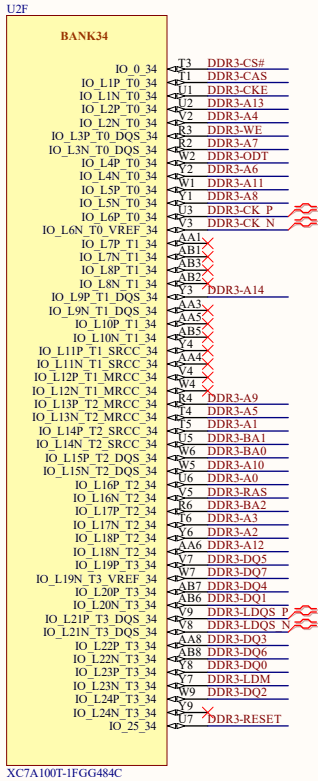


XC7A100T-1FGG484C




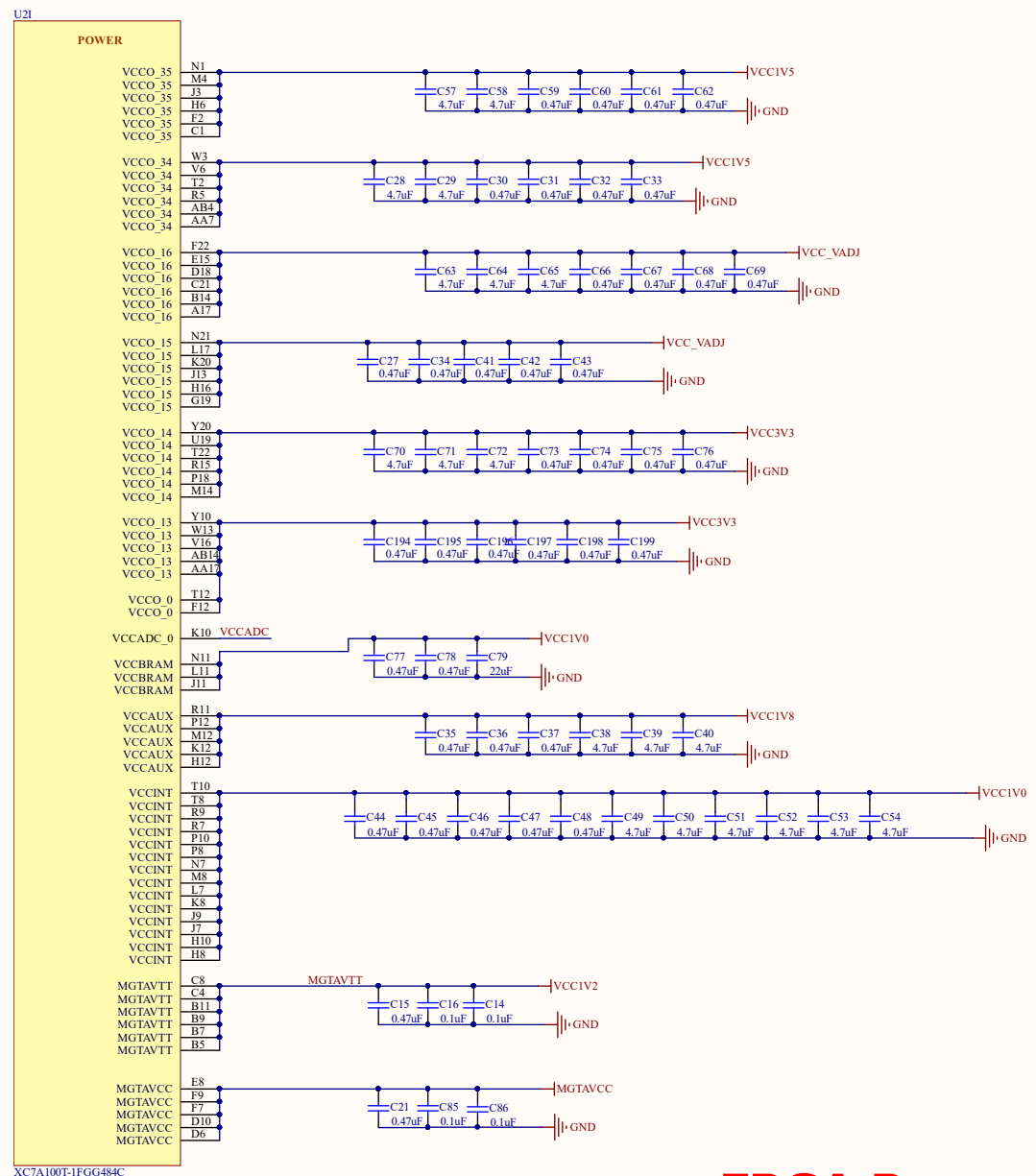
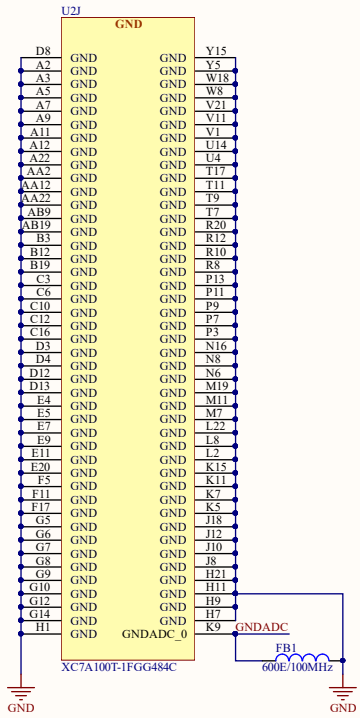
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# FPGA I/O Banks



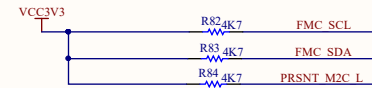
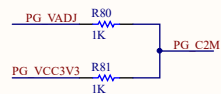
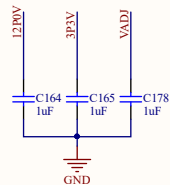
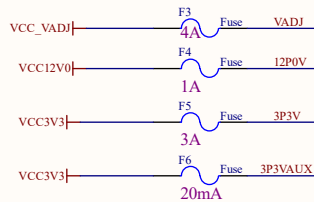
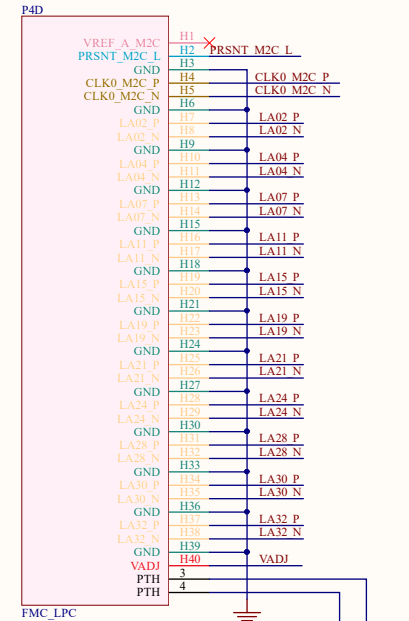
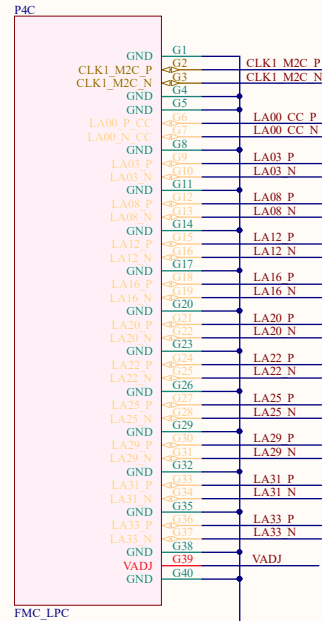
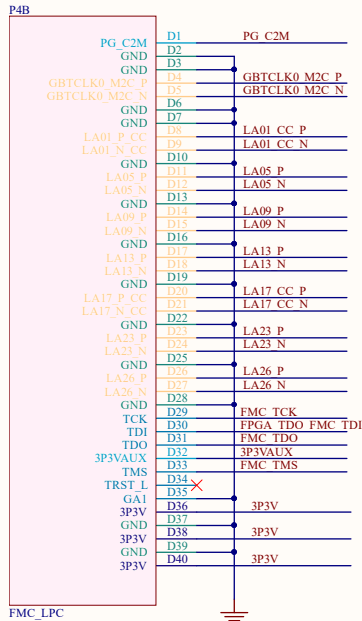
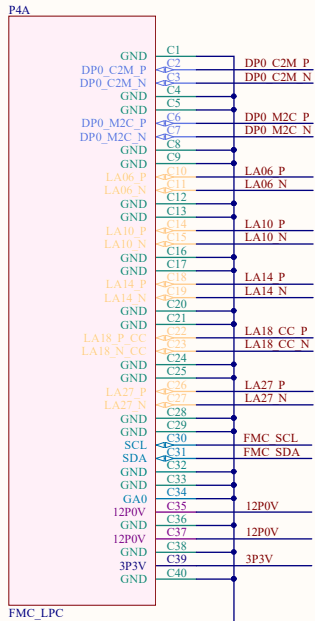
# FPGA DDR3 and PCIeX1 Banks

Title: <b>Tagus</b>	Revision: <b>V2.0</b>	<b>Numato Systems Pvt Ltd</b>		
Size: <b>A3</b>	Project: <b>Tagus.PtjPcb</b>			
Date: <b>5/2/2018</b>	Time: <b>17:16 PM</b>			Sheet <b>5</b> of <b>9</b>
File: <b>FPGA_A_SchDoc</b>				



# FPGA Power

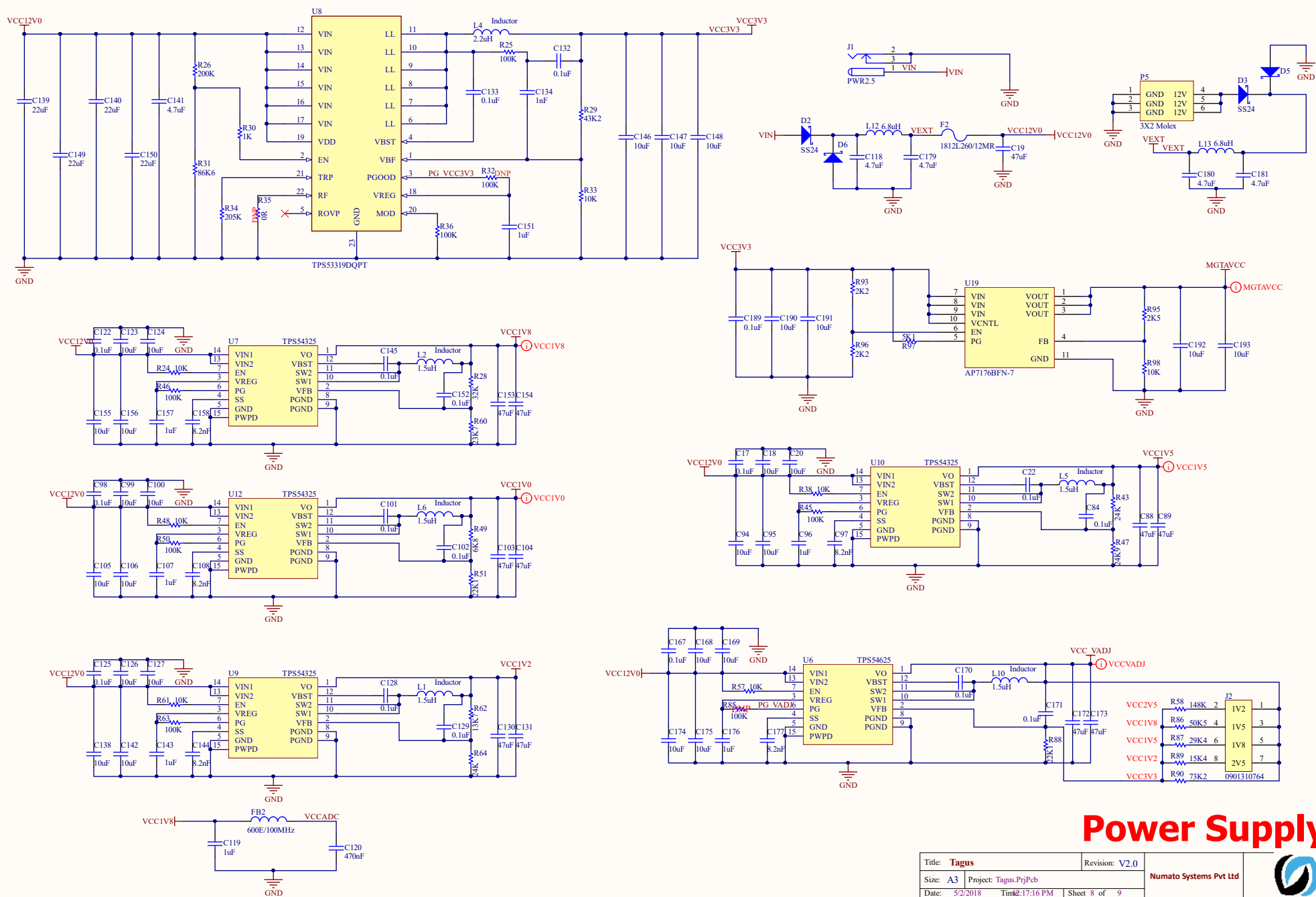
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Size: A3	Project: Tagus.PrjPcb			
Date: 5/2/2018	Time: 17:16 PM			Sheet 6 of 9
File: FPGA_D_SchDoc				




# FMC LPC HEADER

Title: <b>Tagus</b>	Revision: <b>V2.0</b>	<b>Numato Systems Pvt Ltd</b>
Size: <b>A3</b>	Project: <b>Tagus.PrjPcb</b>	
Date: <b>5/2/2018</b>	Time: <b>17:16 PM</b>	
File: <b>FMC_LPC.SchDoc</b>	Sheet <b>7</b> of <b>9</b>	

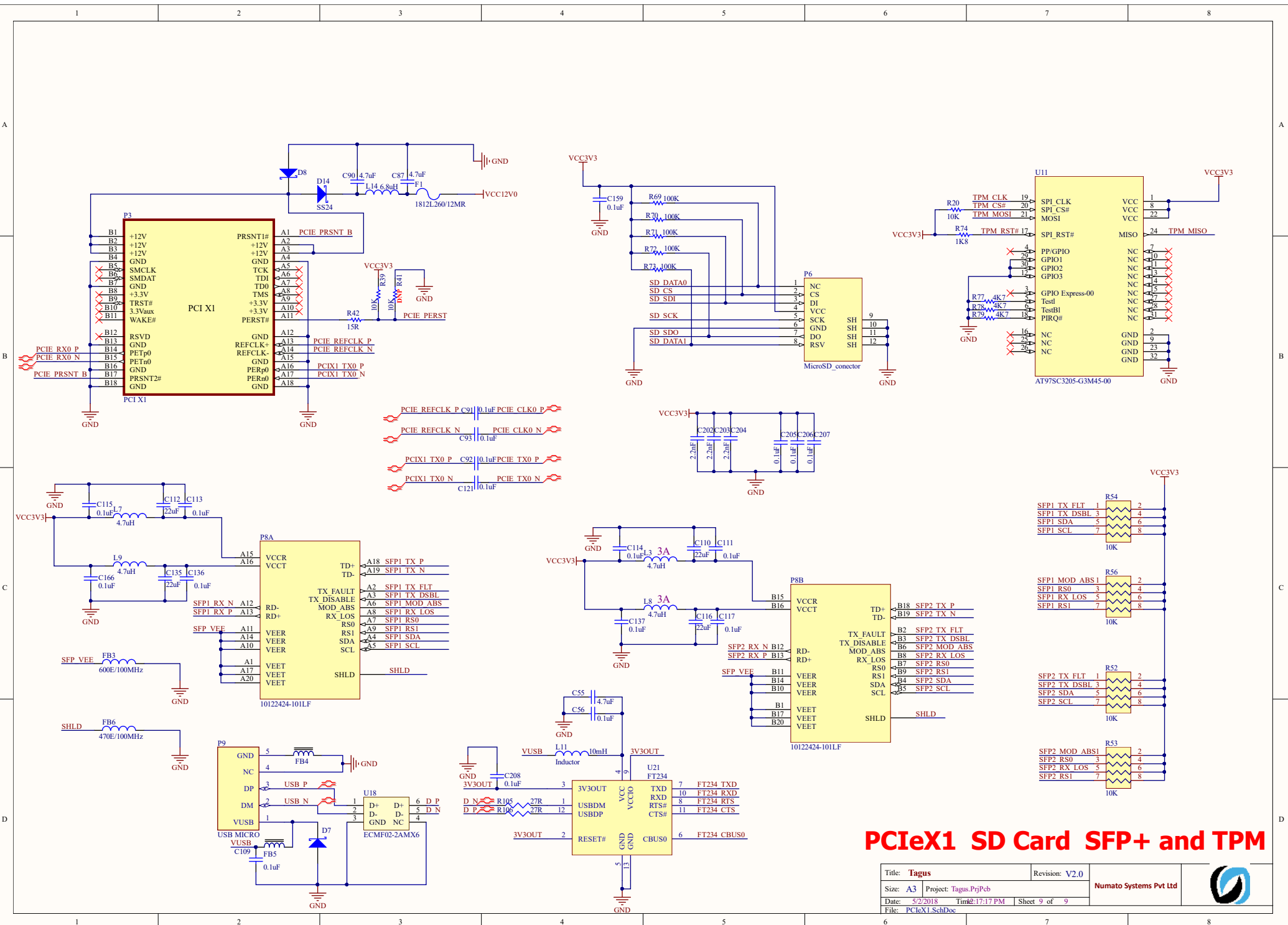





# Power Supply

Title: <b>Tagus</b>	Revision: V2.0	 <b>Numato Systems Pvt Ltd</b>
Size: A3	Project: Tagus.PrgPcb	
Date: 5/2/2018	Time: 17:16 PM	
File: PowerSupply.SchDoc	Sheet 8 of 9	





# PCIeX1 SD Card SFP+ and TPM

Title: <b>Tagus</b>	Revision: V2.0	 <b>Numato Systems Pvt Ltd</b>
Size: A3	Project: Tagus.PrgPcb	
Date: 5/2/2018	Time: 17:17 PM	
File: PCIeX1_SchDoc	Sheet 9 of 9	